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FOREWORD

The proceedings contained herein are compiled and published by the Engineering Department, Naval Weapons Center, as supporting documentation for the 16th Annual Electronics Manufacturing Seminar to be held 19 through 21 February 1992 and sponsored by NWC, China Lake, Calif. This document is a compilation of information that was provided by both nongovernment and government sources.

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Presented are the proceedings of the 16th Annual Electronics Manufacturing Seminar, held on 19–21 February 1992, in Ridgecrest, Calif. The proceedings include the papers presented at the Seminar and cover all aspects of soldering technology and electronics manufacturing. The proceedings are a compilation of information provided by both nongovernment and government sources. The proceedings are published in the interest of furthering communication and broadening awareness of current activities among soldering technology and electronics manufacturing specialists.

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Solder joint reliability
Solder paste flux
Solderability
Solderability inspection
Solderability problem analysis
Soldering attachments
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Spin tinning
Surface-mount assemblies

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INTRODUCTION

The ever-changing, fast-paced technological advances being made today in electronics manufacturing present a challenge to us all. To help meet this challenge, we must work together. This Seminar—the 16th Annual Electronics Manufacturing Seminar—gives us an excellent opportunity to do just that. This Seminar promotes an open exchange of information on all issues of electronics manufacturing. It provides a forum for all persons involved in this technology, whether from government, industry, or academia. Here we can openly discuss these issues and share our ideas. Here we can work together toward our common goal: to improve the U.S. electronics industrial base.

To help make this improvement we must continue to work toward the goals of productivity, producibility, and quality. We must maintain a concerted effort to resolve production-line problems. Then, we must develop process controls and methods to solve them. Because productivity, producibility, and quality are inseparable, it is critical that our designers learn from past problems and that they design for ease of manufacturing. The Navy is continuing to work with industry through the efforts of the Naval Weapons Center at China Lake and the Aircraft Division at Indianapolis.

The continuing goal of the Electronics Production Technology Branch at China Lake is to ensure producibility and quality in electronics manufacturing. We continually evaluate requirements and provide solutions for concerns specific to Naval Weapons Center programs, as well as for government and industry in general. We are continuing to support standardization of specifications requirements, as evidenced through the evolution of requirements from WS-6536E, DOD-STD-2000, MIL-STD-2000, Revision A and B, to MIL-STD-2000, and in providing guidance to industry in developing national standards ANSI/J-STD-001, ANSI/J-STD-002, and ANSI/J-STD-003. Developing technologies, processes, and manufacturing philosophies are providing unique challenges to us all. We are determined to remain in the forefront of this fast-paced world.

We are indeed looking forward to working with you to improve our electronics industrial base. We appreciate your interest in electronics manufacturing and thank you for joining us at this Seminar.

Dr. John W. Fischer, *Head*
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SOLDERABILITY TESTING OF SURFACE MOUNTED COMPONENTS USING THE MICROWETTING BALANCE

by

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ABSTRACT

The theory of the use of the wetting balance, with a solder bath, is discussed, and the limitations of using this technique to measure the solderability of surface mounted components is assessed.

The theory of the microwetting balance, where the solder bath is replaced by a small solder globule, is introduced and the advantages of this method over the solder bath, are discussed. Results obtained using both methods are presented to illustrate the advantages of the microwetting balance method.

The effect of the test conditions and component design on the results is investigated for a number of component types.

INTRODUCTION

The assessment of component solderability as a routine part of soldering process control, reduces the soldering defect rate and enhances the quality of the finished product. It also facilitates the use of cheaper, environmentally-friendly soldering materials, such as 'no-clean' fluxes and solder creams.

Quantitative solderability test methods for leaded components have been available for many years (ref 1, 2, & 3), but attempts to extend these tests to surface mounted components, have proved rather unsuccessful. The very small size of both the component and the terminations, has made physical measurements extremely difficult.

The wetting balance method for assessing component solderability appeared the most likely method to produce a quantitative test method for surface mounted components, but early work using the conventional wetting balance with a solder bath, produced poor results (ref 4).

There was clearly a need to improve both the sensitivity and the spacial resolution of the method. The microwetting balance, where the solder bath is replaced by a small globule of molten solder, gives immediate improvement in both these areas. This enables quantitative solderability measurements to be made on most types of leaded and leadless surface mounted components.

THE SOLDER BATH METHOD

The wetting balance is used to measure the resulting forces of buoyancy (Archimedes), and changing surface tension, as molten solder wets an immersed specimen. The forces acting on the specimen are shown in figure 1 where a vertical plate has been immersed into a solder bath.

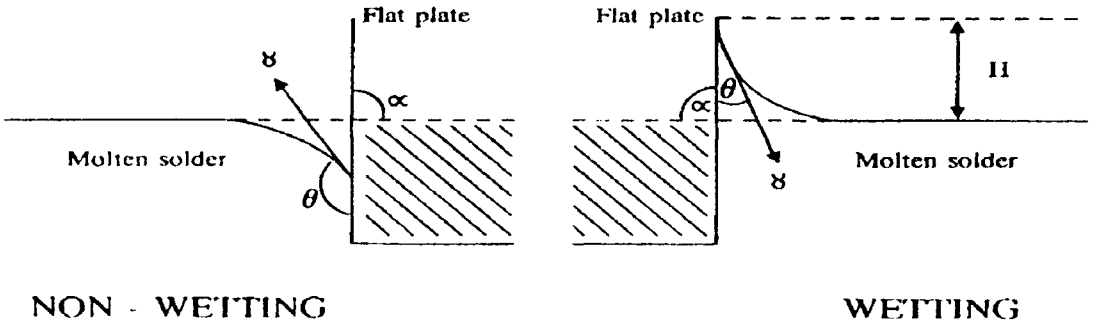

FIGURE 1. The Wetting Forces Acting on an Infinite Plate

The wetting balance is normally used in the rapid dipping or stationary mode. This is where the component is immersed at a fairly high immersion speed so that initially no wetting occurs. The left hand side of figure 1 shows a flat plate after immersion and before wetting commences.

The molten solder is depressed by the unwetted plate giving a contact angle greater than 90° between the vertical side of the specimen and the liquid surface. This results in a vertical or rejecting force from the solder surface tension. Once the plate starts to wet, the liquid solder rises up the vertical sides and the contact angle reduces.

As the solder rises above the level of the bath, the surface tension force starts to act downwards and pull the plate down into the solder bath. The wetting balance monitors this changing surface tension force, as the contact angle changes from non-wetting to wetting, and by analysing the force against time curve, the solderability can be assessed (refs 1, 2 & 3).

The changing surface tension force is superimposed on top of the buoyancy, or Archimedes force, created by the displacement of a volume of molten solder as the plate is immersed. This force remains constant during the test, and can be equated to the measured force when the contact angle is 90°.

The vertical force measured by the wetting balance is given by:

$$F = \gamma P \cos \theta - g \rho V \qquad (1)$$

where

γ =	surface tension of molten solder	(0.4 mN mm^{-1})
P	specimen perimeter	(in mm)
θ =	contact angle	
g =	gravitational acceleration	(9.81 x 10^3 mm s^{-2})
ρ =	solder density	(8mg mm^{-3})
V =	specimen immersed volume	(mm^3)

In practice the speed of wetting is assessed by measuring the time to reach some reference point, such as the buoyancy line, and the extent of wetting is measured by the magnitude of the wetting force.

For a leaded component the vertical force is limited by the solderability of the component. The height of rise of the solder meniscus is given by the elastica curve, derived by Rayleigh, to describe the shape of the solder meniscus(Equation 2).

$$H = \sqrt{\frac{\gamma}{\rho g}} \times 2\,\mathrm{SIN}\ \frac{(\alpha - \theta)}{2} \qquad (2)$$

Where α, is the immersion angle between the vertical side of the component and the solder surface.

If we assume perfect wetting where the contact angle tends to zero, then H, the height of rise of the solder meniscus above the solder bath, could be as high as 3.2 mm.

While this presents no problem for most leaded components, very few surface mounted components have a free lead length of over 3 mm to test. This results in the height of solder rise being limited not by the solderability, but by the physical length of the solderable termination.

Even if we assume a more normal contact angle of 40°, the predicted rise height would be 2 mm which is still higher than the termination length on many chip components.

The above calculations all assume that we are wetting an infinite plate. In practice, this is not the case, and the result of dipping a termination or chip component into molten solder is to introduce a curvature into the plane of the solder surface. This further limits the height of solder rise, and although this helps the situation, it does not reduce the theoretical maximum rise height to less than the termination length found on many chip components.

THE MICROWETTING BALANCE METHOD

a) Reducing the Rise Height

In order to use the wetting balance to assess the solderability of surface mounted components, we need to reduce the height of rise of the solder meniscus so that the vertical wetting force can be used as a measure of the extent of wetting. If we look at equation 2, we can see that we could reduce the height of rise, H, by reducing the entry angle, α. Unfortunately, this cannot be achieved by immersing the termination at an angle as the reduced entry angle on one side is cancelled by the increased entry angle on the other side.

A practical solution to this problem is to curve the surface of the solder. This is achieved by using a solder globule in place of a solder bath. The solder globule is obtained by melting a solder pellet on a circular iron pin, set in a heated aluminium block. The solder will only wet the iron, and hence the solder forms a stable, well defined molten globule. This technique is already well known in the standard globule test (refs 2, 5).

Figure 2 shows how the curvature of the solder globule affects the entry angle. If we dip a 1206 capacitor vertically into a 200 mg solder globule, we find the entry angle is reduced from 90° to 70°. If we use equation 2 to evaluate the theoretical maximum rise height, we find the height reduced from 3.2 to 2.6 mm, and by taking a more normal contact angle of 40°, we obtain a height reduced from 1.9 to 1.2 mm. If we remember that the curvature introduced by the small radius of curvature will further reduce the rise height, we are now approaching a theoretical rise height closer to the termination length available on many chip components.

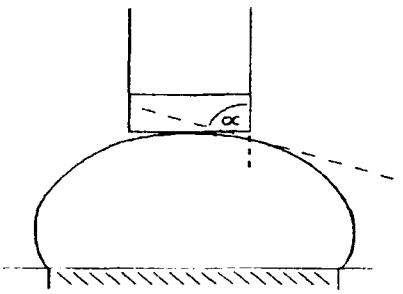

FIGURE 2. Curving the Solder Surface to Reduce the Entry Angle

b) The Wetting Forces

Figure 3 shows the wetting curve obtained from a 1206 chip capacitor when one end was tested. The results were obtained using a solder bath and a 200 mg solder globule. In both cases the termination was immersed 0.1 mm into the solder.

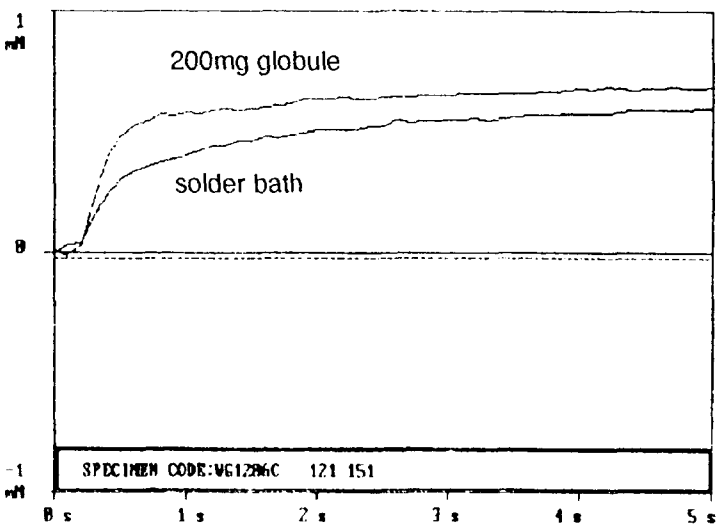

Figure 3 Wetting curves obtained from a 1206 chip capacitor

The microwetting balance not only produces a wetting force limited by the solderability, but also produces a larger wetting force which gives a greater resolution between different levels of solderability.

It is not immediately obvious why the solder globule produces a higher wetting force. It has been suggested that the increased force is due to the filling of the space beneath the underside of the component with solder. However, if we look at figure 4, which shows a scale drawing of a 1206 capacitor dipped 0.1 mm deep into a 200 mg solder globule, we can see that the space is already filled by the time the immersion depth has been reached.

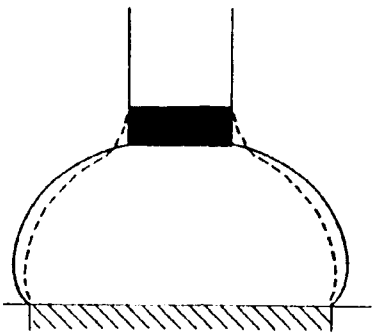

FIGURE 4. Distortion of the Solder Globule During Wetting

It appears that the gain in wetting force, obtained with the solder globule, is due to the distortion of the solder globule as the termination solders, shown by the dotted line in figure 4. This distortion is working against the surface tension force which is trying to maintain the solder globule with the smallest surface area. The theoretical calculation of this force is not fully evaluated, and computer modelling is currently being carried out to resolve this problem.

c) The Solder Globule Size

Evaluation of the microwetting balance method has so far concentrated on two sizes of solder globule - a 200 mg solder globule on a 4 mm iron pin and a 25 mg globule on a 2 mm iron pin.

A major advantage of the microwetting balance method is that individual leads on a multileaded device can be tested much more easily than with the solder bath. So far the 200 mg globule has been used to test the larger chip components and the individual leads on SOIC, PLCC and QFP devices. The 25 mg globule has been used to test small chip devices and SOT-23 leads.

Figure 5 shows the wetting curves obtained on an 0603 capacitor using a solder bath, a 200 mg solder globule, and a 25 mg solder globule. The increased resolution of the microwetting balance method is immediately obvious, and the use of the smaller globule size produces a further increase in the wetting force.

The increased wetting force obtained with the 25 mg solder globule has been attributed to the greater distortion force exerted on the 25 mg solder globule.

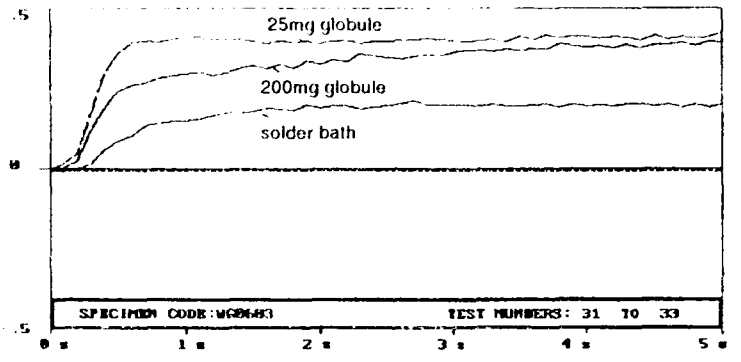

FIGURE 5. Solder Bath and Microwetting Balance Curves on a 0603 Capacitor

d) Spacial Resolution

The microwetting balance allows individual leads to be tested on a multileaded device, and equipment is already available that allows the solder globule to automatically advance along the leads of a multileaded device. This now makes it a very quick, simple operation to test the leads on one side of a multileaded device.

If we assume that the solder globule forms a hemisphere, we can calculate the globule size required to enable individual leads to be tested on a multileaded device. This is not strictly true, but is an adequate approximation (ref 6).

Figure 6 shows the desired globule position when an immersion depth of 0.1 mm is used.

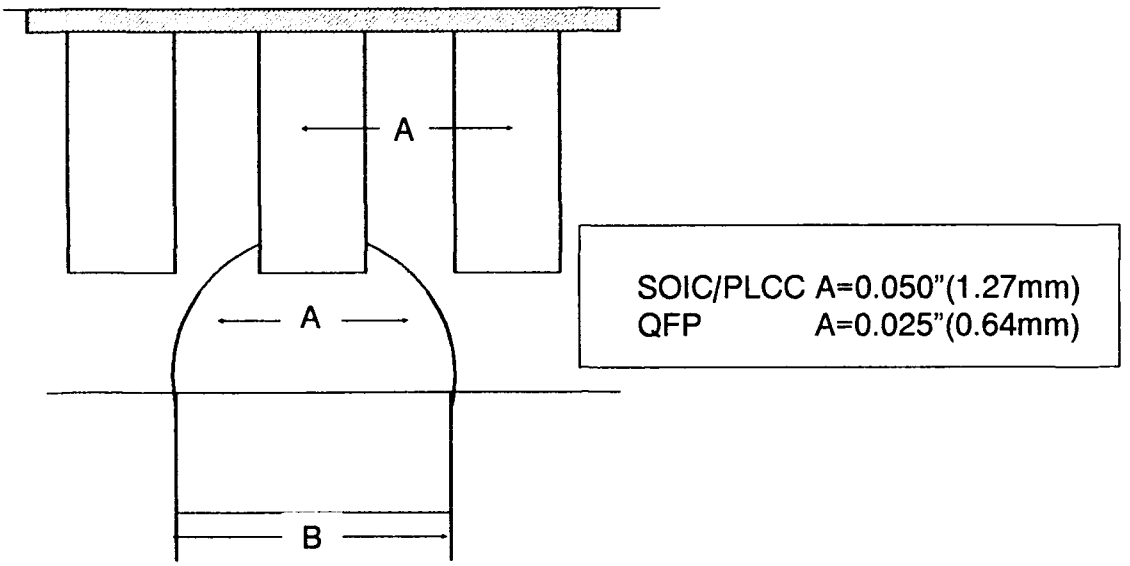

FIGURE 6. Solder Globule Size Required to Test Individual Leads

The lead spacing on a PLCC or SOIC device would allow a 4 mm pin to be used, but a QFP device would require a 1 mm iron pin. This would be practically quite difficult to manufacture as the iron pin has to be a press fit in the aluminium to obtain good heat transfer, and the volume of the solder globule would be inadequate to both heat the QFP lead and solder up the lead.

It is normal practice to perform solderability testing with a non-activated test flux (Type R). The result of this practice is that at the end of the test, the flux has insufficient activity to remove the oxide film formed on the solder surface, and a spike of solder remains on the tested lead as the solder globule is pulled away. For a PLCC lead, the amount removed is approximately 1.5 mg, and for a QFP, the amount removed is approximately 0.18 mg.

This solder spike will interfere when the adjacent lead is tested, unless the globule diameter is further reduced. In order to maintain sufficient solder volume to both heat and solder the leads, it has been found necessary to test PLCC, SOIC and QFP leads with a 200 mg solder globule.

When testing components with 0.50 in (1.27 mm) lead spacing, alternate leads are bent back away from the test area, and when testing leads with 0.025 in (0.64 mm) spacing, two leads have to be bent back between the tested leads. Although this may not be the ideal situation, it does provide the advantage that a single 200 mg solder globule can be used to test all the leads on one side of a component. The test equipment automatically advances to the next lead after each test, only requiring fresh flux to be added to the globule.

e) Thermal Demand

Solderability test methods generally measure the combined effects of the wettability of the termination, and the thermal demand of the lead. The microwetting balance technique is particularly sensitive to the thermal demand of the lead. Figure 7 illustrates an extreme case showing the results of testing an outer lead and a centre lead on a SOT-89 device.

The centre lead has a much greater mass than the two outer leads and so requires much longer to reach soldering temperature which is immediately obvious from the wetting curve. Once soldering starts, the wettability of both the outer and centre lead was very similar.

The sensitivity of the microwetting balance method is so good that thermal differences have even been observed at the corner leads of SOIC devices (ref 7).

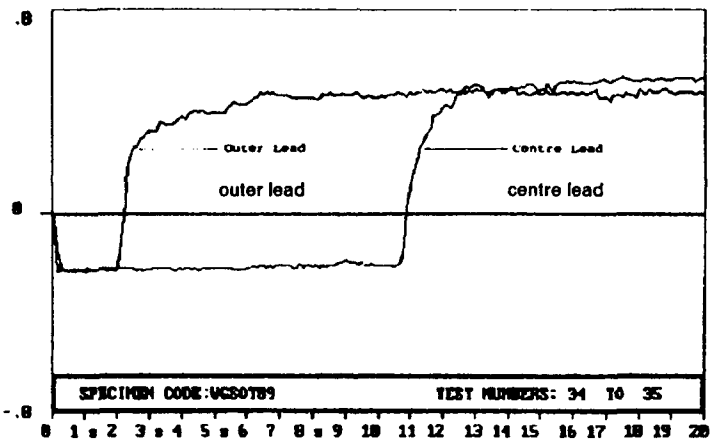

FIGURE 7. Microwetting Balance Test on a SOT-89 Device

f) Artificial Ageing

To test the sensitivity of the microwetting balance to the effects of ageing on a component, an 0603 capacitor was aged in dry air at 155°C for 16 hours and for 72 hours, and the results compared.

The resulting wetting curves shown in figure 8 are each the mean of five tests. The degradation of the solderability, as the ageing time increases, is quite clear. It would be a fairly simple matter to select a value, such as the force at 2 seconds, to distinguish between the different levels of solderability, but to set a solderability requirement for a component to be used on a production line, is a much more difficult task.

The method is clearly sufficiently sensitive to distinguish between different levels of solderability, and work to determine the level of solderability required to produce a reliable soldered joint is currently being carried out.

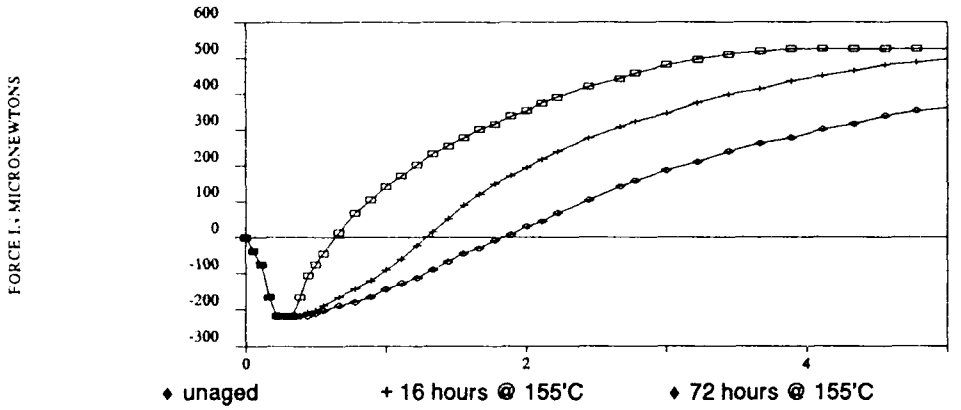

FIGURE 8. Microwetting Balance Curves Showing the Effect of Artificial Ageing

g) Test Flux

Solderability testing has traditionally been performed using a non-activated (Type R) flux. The reason for this has been to build a safety margin into the test method where only a small sample may be tested from a large batch.

We have already seen that using a non-activated flux has presented problems with the microwetting balance where the flux is not sufficiently active at the end of the test to allow the solder to break away from the termination without leaving a spike. There is also evidence from video photographs that the non-activated flux does not fully clean the surface of the solder globule, and in fact, forms a polymerised crust over the solder globule, which is not easily penetrated by the component termination.

By adding 0.5% halide to the test flux, these problems can be overcome, but the sensitivity of the method to different levels of solderability is reduced.

Table 1 shows the forces measured at 2 and 5 seconds from a test series performed on a 1206 capacitor with non-activated and activated flux. The problem with the non-activated flux is shown by the greater spread in the results, believed to be aggravated by the failure of the flux to fully clean the solder globule during the complete test cycle, usually 5 seconds.

The improved efficiency of the activated flux is shown by the higher wetting force obtained at 2 and 5 seconds, and by the reduced spread in the results. The reduced spread in the results is attributable not only to the improved efficiency of the flux cleaning the termination, but also the improved cleaning of the solder globule.

Work is still continuing to evaluate the best fluxing technique to use to obtain consistent results and maintain the sensitivity of the method to different levels of solderability.

TABLE 1. Wetting Forces in microNewtons with Pure Rosin and Halide Activated Rosin

Pure Rosin			Pure Rosin + 0.5% Halide	
	F2	F5	F2	F5
Test No1	232	434	Test No7..... 541	629
Test No 2	387	434	Test No 8.... 424	614
Test No 3	279	356	Test No 9.... 585	746
Test No 4	372	496	Test No 10.. 512	658
Test No 5	294	372	Test No 11.. 453	570
Test No 6	372	449	Test No 12.. 556	687
Mean	323	424	512	651
Standard Deviation	58	47	57	56
% Deviation	18	11	11	9

SUMMARY

The work to develop a test method for SMD components using the wetting balance has been a major project at Multicore Solders during the last five years. New equipment has been developed to overcome the technical difficulties and to improve the ease of operation. The method can now be readily applied to a wide range of surface mounted devices to determine the thermal and wetting properties of the terminations.

During the last two years this work has formed part of a much wider collaborative project with Philips, Siemens, and the UK National Physical Laboratory, with the assistance of a BRITE Research Award from the European Community. The aim of this project is not only to produce a solderability test method for surface mounted devices, but also to correlate solderability test results with component termination finishes and surface conditions, and to relate this information to the performance of production soldered assemblies.

The aim of this paper is to introduce the microwetting balance technique and show some of the advantages of the method over previous techniques.

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John Porter is the Equipment Division Manager at Multicore Solders Limited. He joined Multicore Solders in 1969, working on solders and fluxes, and in 1976 took over responsibility for solderability test equipment. John holds a BS degree in Chemistry and is a qualified chemist.

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CIRCUIT CARD ASSEMBLY SOLDERABILITY

PROBLEM ANALYSIS

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ABSTRACT

During March, 1991, ITT A/CD Rockledge began a Circuit Card Assembly (CCA) solderability investigation in an effort to reduce the CCA wavesoldering defect rate.

Design of experiment techniques were utilized to optimize the wave soldering process. Best level wavesolder machine settings were identified for process robustness against Printed Wiring Boards (PWB's) of varying age.

The predominant wavesoldering defects were identified as PWB solderability problems. This paper will show how A/CD Rockledge worked with a PWB supplier to achieve a thicker tin-lead plating on PWB plated through holes to enhance solderability.

OBJECTIVE

To reduce the number of wavesolder defects per Circuit Card Assembly (CCA) measured in parts per million. Some CCA's required two passes through the wavesolder system. The rework of soldered connections is costly, may compromise CCA reliability and adversely impacts circuit card assembly cycle time.

GOALS

One of the goals of the study was to select the best wavesolder process levels using Design Experiment Techniques (Taguchi) to improve the defect rate of all PWB's (old and new) providing increased robustness against date codes of varying age and solderability.

Another goal was to establish a better understanding of ITT A/CD drawing specifications and requirements for suppliers, that they may provide high reliability, solderable, printed wiring boards.

Another goal was to assist suppliers in conducting Taguchi experiments to define process capabilities and also maintain product quality by the implementation of statistical process control.

Yet another goal was to establish a procedure for A/CD Rockledge to procure and use PWB's in a timely manner.

WAVESOLDER PROCESS EVALUATION

DESIGN OF EXPERIMENT

Due to the complex nature of the wavesolder process and material used in its operation, brainstorming was used to represent all departments directly involved with day-to-day operation of the wavesolder process. All participants were chosen for their expertise and experience with the wavesolder system.

All participants actively participated and clearly defined numerous probable areas of control and difficulties encountered over the course of their operation. Process control concerns, process variables and parameters for the experiment were developed.

Process Description

The wavesoldering operation at the ITT Aerospace/ Communications Division Rockledge Facility, is typical of a high-reliability (Mil-Std-2000) process. Prebaking multi-layer PWB's prior to wavesolder is a concern to minimize outgassing and delamination. The flux used in the process is mildly activated rosin (RMA) flux. The Electrovert wavesolder machine consists of a conveyor transporting the CCA's across the foam fluxer, infrared preheaters and over the dry LAMBDA solder wave. Cleaning subsequent to wavesoldering is accomplished using a Detrex in-line wire link conveyor cleaner utilizing Freon TMS as the solvent to remove flux residue.

The inspection of wavesoldered connections follows the criteria of Mil-Std-2000. Inspection tally sheets are used to record the wavesolder defects by category and CCA serial number. This inspection data serves as the basis for calculating the wavesolder defect rate (in parts per million, PPM) and was used as data for the wavesolder Taguchi experiment.

Controllable and Noise Factors

The controllable factors are shown in Table 1 as eight inside columns in a modified L18 orthogonal array. The noise factors for the experiment consisted of three outer factor columns. The outer factor columns were established to evaluate the relative solderability of various printed wiring board date codes. It was believed that the age of PWB's would have an affect on solderability due to the formation of intermetallic compounds (IMC) in the plated through holes over time.

Each factor column was assigned a PWB date code. Factor 1 consisted of a six month old PWB date code. Factor 2 consisted of the same six month old date code, but was reprocessed using a solder reflow method to "rejuvenate" the tin-lead plating on the plated through holes (PTH's). This procedure was done to remove surface contamination from the PTH's and to provide a solderable surface theoretically not having IMC's at the surface of the PTH's. It was theorized that the rejuvenation process would improve wetting and reduce pits, holes and voids caused by foreign material (permanent soldermask) on pads and in plated through holes. Factor 3 consisted of a new eight week old date code PWB.

Three iterations of each experiment were conducted.

TABLE 1. Orthogonal Array

MODIFIED L-18 ARRAY

	FLUX SOLIDS-%	PRE-HEAT TEMP-Deg F	SOLDER TEMP-Deg F	TOP SIDE FLUX-Y/N	DEPTH IN WAVE-%	DWELL TIME-SEC.	BAKE TIME-HOURS	OMEGA WAVE-%	OUTER FACTOR COLUMNS		
EXPERIMENT NUMBER	A	B	C	D	E	F	G	H			
	1	2	3	4	5	6	7	8	F1	F2	F3
1	1	1	1	1	1	1	1	1	1	2	3
2	1	1	2	2	2	2	2	2	4	5	6
3	1	1	3	2	3	3	3	3	7	8	9
4	1	2	1	1	2	2	3	3	10	11	12
5	1	2	2	2	3	3	1	1	13	14	15
6	1	2	3	2	1	1	2	2	16	17	18
7	1	3	1	2	1	3	2	3	19	20	21
8	1	3	2	2	2	1	3	1	22	23	24
9	1	3	3	1	3	2	1	2	25	26	27
10	2	1	1	2	3	2	2	1	28	29	30
11	2	1	2	1	1	3	3	2	31	32	33
12	2	1	3	2	2	1	1	3	34	35	36
13	2	2	1	2	3	1	3	2	37	38	39
14	2	2	2	2	1	2	1	3	40	41	42
15	2	2	3	1	2	3	2	1	43	44	45
16	2	3	1	2	2	3	1	2	46	47	48
17	2	3	2	1	3	1	2	3	49	50	51
18	2	3	3	2	1	2	3	1	52	53	54

WAVESOLDER PROCESS EVALUATION

Quality Characteristic

The quality characteristic for the experiment was identified as the acceptance or rejection of the soldered connections in complaince with the criteria of Mil-Std-2000.

The quantity of rejectable solder conections was logged by defect category and serial number by Mil-Std-2000 category D inspectors using a post solder inspection tally sheet.

EXPERIMENTAL RESULTS

An Anova Table was generated, resulting in the Anova Table in Table 2.

TABLE 2. Anova Table

	Source FACTORS	Pool (*=S MS)	Df Degrees of Freedom	S VARIATION	V VARIANCE	F F' TEST	S' <POST POOL>	rho% CONTRIBUTION
A	Flux Solids	[N]	1	142.04142	142.04142	8.42093	126.17376	7.26
B	Preheat Temp.	[Y]	2	67.75146	33.87573			
C	Solder Temp.	[Y]	2	33.09844	16.54922			
D	Top Side Flux	[N]	2	228.88509	114.44254	6.78473	196.14977	11.31
E	Depth In Wave	[N]	2	147.50239	73.75119	4.37234	113.76707	6.59
F	Dwell Time in Wave	[N]	2	861.75864	430.87932	25.54470	828.02332	48.00
G	Bake Time (oven)	[Y]	2	5.62361	2.81180			
H	Omega Wave	[N]	2	210.08220	105.04110	6.22737	176.34688	10.22
AXB		[Y]	2	28.46778	14.23389			
e1		[Y]	0	0.00000				
e2		[Y]	0	0.00000				
(e)			8	134.94129	16.86766		286.75023	16.62
Total (Raw)		[-]	17	1725.21100	101.48300			

Level averages were calculated. Response graphs were printed for all factors as shown in Figures 1, 2, 3.

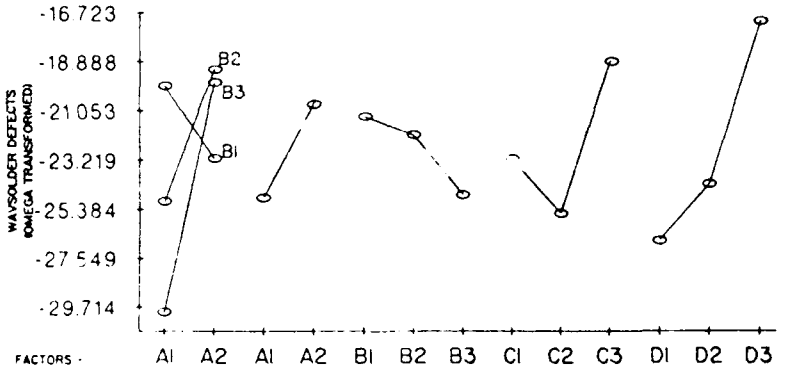


FIGURE 1. Response Graph

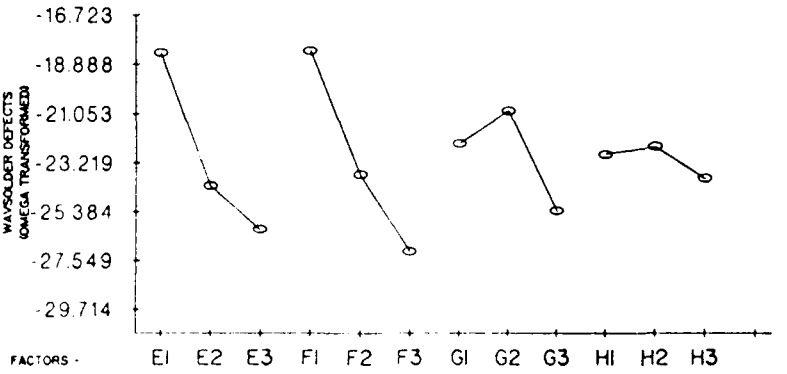


FIGURE 2. Response Graph

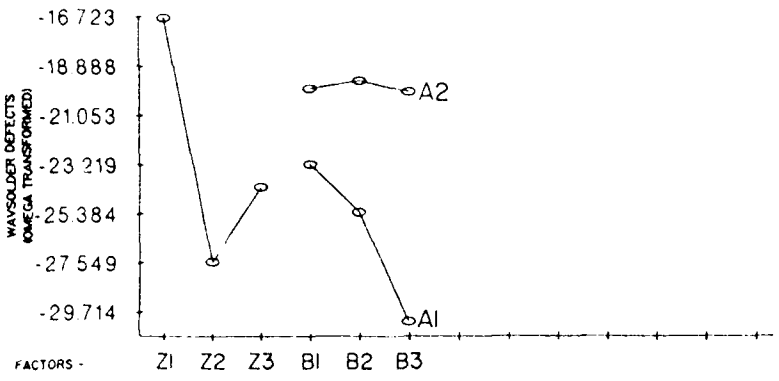


FIGURE 3. Response Graph

Selection of Optimal Levels

Level averages and response graphs were reviewed to select optimal levels for all factors shown in Table 3.

TABLE 3. Selection of Optimal Levels

	FACTOR	OPTIMAL LEVEL
A	FLUX SOLIDS	A1 25%
B	PREHEAT TEMPERATURE	B2 220°F
C	SOLDER TEMPERATURE	C2 500°F
D	TOP SIDE FLUX	D1 ADDITIONAL FLUX - YES
E	DEPTH IN WAVE	E3 100%
F	DWELL TIME	F3 5 SECONDS
G	BAKE TIME	G1 4 HOURS
H	OMEGA WAVE	H3 40%
Z	PWB DATE CODE	Z2 REJUVENATED PWB

Process Estimate

Process estimates and confidence intervals were calculated based on the experimental solder defect data for current and optimal operating levels.

Current Operating Levels 684 PPM to 117,700 PPM

Optimum Operating Levels 4 PPM to 537 PPM

Present Process Average	10,089 PPM
Optimum Process Average	46 PPM
Potential Estimates Improvement	10,043 PPM

In practical terms, the "present" average process defect rate as of WW 14 was 6800 PPM. The potential improvement would therefore be 6754 PPM or a reduction of 3.7 defects per board.

CONFIRMATION EXPERIMENT

A confirmation experiment was conducted on April 12, 1991. 18 circuit card assemblies (6 old, 6 new, and 6 rejuvenated) withheld from the experiment lot were wavesoldered using optimum levels for factors A through H.

Following the wavesoldering process, the boards were inspected and the data recorded on inspection tally sheets.

Of particular interest was the fact that pits, holes and voids and poor wetting defects were significantly reduced. The only boards indicating these types of defects were the old date code PWB's.

The summary of the confirmation experiment is shown in Table 4.

TABLE 4. Confirmation Experiment Summary

OPTIMAL PROCESS ESTIMATE	CONFIRMATION EXPERIMENT RESULTS	
	OLD DATE CODE PWB'S (Z1)	3869 PPM
4 PPM TO 537 PPM (USING Z2 PWB'S)	REJUVENATED PWB'S (Z2)	1488 PPM
	NEW PWB'S (Z3)	1190 PPM
	COMPOSITE	2182 PPM

IMPROVEMENTS DEFINED

The wavesolder process experiment resulted in a reduction of wavesoldering defects for all printed wiring board date codes. However, the experiment data indicated a significant amount of variability, with old date code PWB's. A process estimate for optimum settings and old PWB's predicted a range from 300 PPM to 8700 PPM. Following the selection and implementation of best level process settings, production continued to encounter a large quantity of PWB's with old date codes maintaining the defect rate at approximately 4500 PPM. The original two largest defects (pits, holes, and voids and poor wetting) were quite prominant. A comparision between old settings and optimum settings is shown on the next page.

Before Optimum Settings	After Optimum Settings	
	Confirmation Data	Production Data
6800 PPM (3.8 defects)	2182 PPM (1.2 defects)	4500 PPM (2.5 defects)

From the experiment, it was observed that rejuvenation of the tin-lead plated surfaces of a PWB had a definite impact on reducing of soldering defects, especially pits, holes and voids and some reduction of poor wetting. New PWB date codes also exhibited superior wavesolder results. Further investigation was conducted concerning rejuvenated PWB's, refinement of a PWB specification for suppliers and procuring new printed wiring boards with thicker plating to provide a solderable PWB after a three month storage time.

Rejuvenated PWB's

A/CD Rockledge Manufacturing Engineering identified a supplier for rejuvenating the tin lead surfaces on PWB's. The objective of the rejuvenation was to rejuvenate old printed wiring boards in stock until new PWB's would be available for all part numbers. The rejuvenation was viewed as a short term effort to purge approximately 10,000 PWB's with old date codes.

During the first week of May, 1991, (Work Week 18), 150 old PWB's were rejuvenated, populated, wavesoldered and inspected. The rejuvenation process reduced the defect rate of old PWB's from 4639 PPM to 1357 PPM. Refer to Figure 4. The rejuvenation process virtually eliminated pits, holes, and voids and significantly reduced de-wetting, non-wetting and poor wetting. Refer to Figure 5.

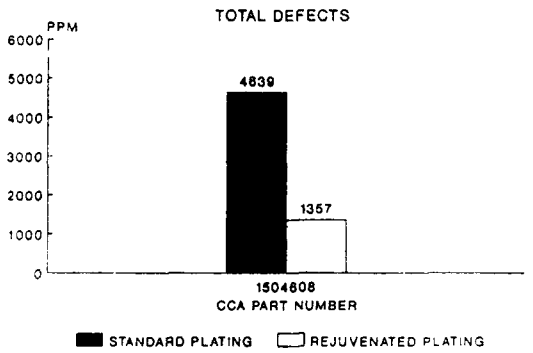


FIGURE 4.
CCA Solderability - Standard vs Rejuvenated PWB's

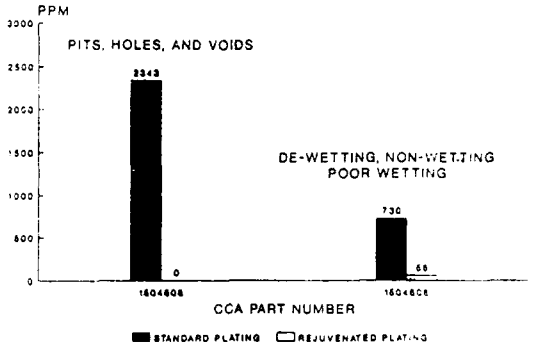


FIGURE 5.
CCA Solderability - Standard vs Rejuvenated PWB's

Based on the results of the pilot lot of rejuvenated PWB's, rejuvenation of PWB's with old date codes began for production during late June, 1991.

New, Thicker Plating PWB's

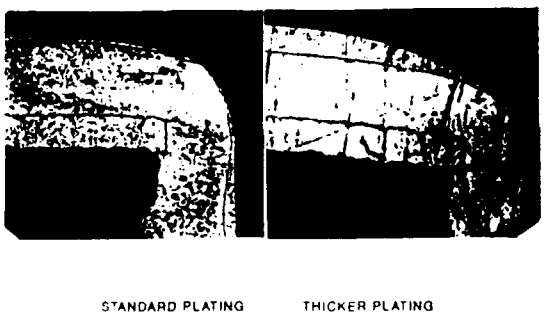
At the start of the PWB solderability investigation, a need to better define the requirements for highly solderable PWB's was identified. Following the initial experiment, the need for guidelines to procure and use new PWB's in a timely manner became more obvious. During April and May, 1991, two PWB suppliers agreed to follow the guidelines of the A/CD Rockledge PWB solderability specification.

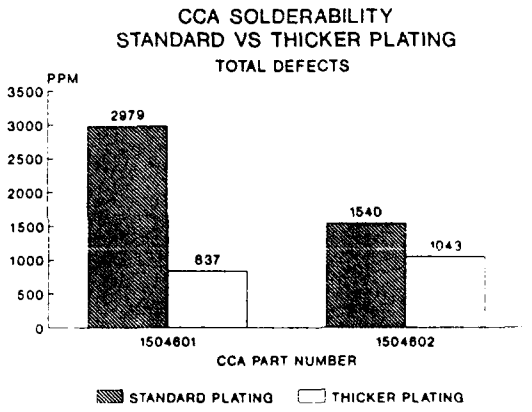
In addition to restrictions on the time from reflow to delivery, one supplier agreed to investigate increasing the tin lead plating thickness after reflow, in an effort to improve solderability.

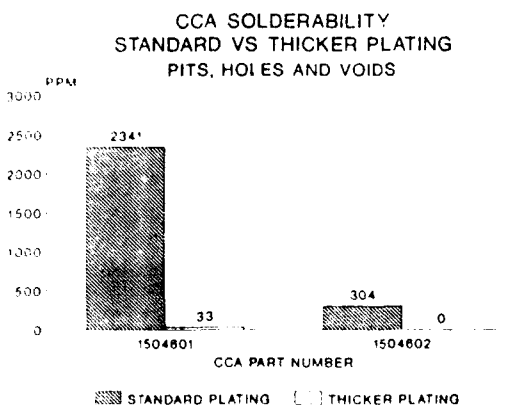
It is believed that thicker tin-lead plating provides robustness against aging and improves the solderability within 90 days after tin-lead reflow by alleviating the presence of intermetallic compounds (IMC) on the surface of the plated through holes (especially on the knees).

By early May 1991, the supplier provided samples of the thicker tin-lead plated PWB's. The supplier set plating thickness targets of .000850" as plated and .000700" to .001000" after reflow as measured at the crest on the plated through hole pad and barrel wall. This also improved the thickness of the plating on the knee of the plated through hole.

A quantity of 125 PWB's of each of two part numbers was populated, wavesoldered and inspected during early May, 1991 (Work Week 18). The new, thicker plating PWB's reduced the wavesolder defects from 2979 PPM to 837 PPM for one part number and from 1540 to 1043 for the other part number (using optimum process settings). The new, thicker plating PWB's virtually eliminated pits, holes and voids and significantly reduced de-wetting, non-wetting and poor wetting. Refer to Figure 6.







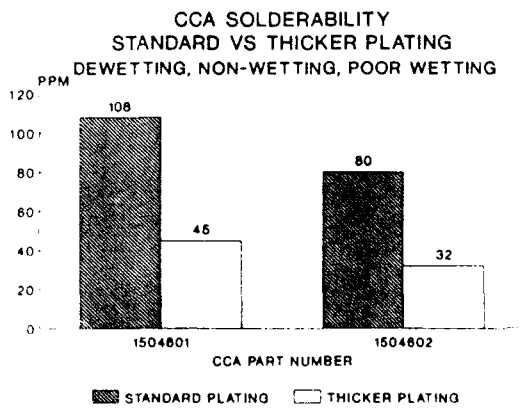


FIGURE 6. CCA Solderability - Standard vs Thicker Plating on PWB's

The supplier continued to fabricate the thicker plating PWB's and demonstrated the ability to deliver the PWB's to ITT A/CD within three to four weeks from the date of reflow.

Perturbations with the preceding supplier's process were detected late in May and early June, 1991 (Work Week 22 and 23). The supplier was notified and corrective action was taken by July 1991. ACD Rocklege Manufacturing Engineering visited the supplier during late July, 1991 (Work Week 31) and conducted a brainstorming session in preparation for a Taguchi experiment on the supplier hot oil reflow process to be conducted during September and October, 1991.

SUPPLIER PROCESS EVALUATION

After review of the PWB supplier's process by ITT A/CD, a joint decision was made to evaluate the supplier's hot oil fusing process. This process appeared to be in need of optimization. Proper control of this process would have a definite impact on the reflowed tin lead plating thickness on pads of PWB's after fusing.

Previous investigation indicated that a plating thickness of 700 to 1000 microinches minimum after fusing was desirable for optimum PWB solderability, especially when PWB's were stored 90 days or more before soldering. More than 1000 microinches was not found to be detrimental (providing hole diameters met the drawing requirements), but did not provide any significant additional benefit.

DESIGN OF EXPERIMENT

ITT A/CD Manufacturing Engineering and ACI personnel conducted a brainstorming session to define controls and areas of difficulty encountered during hot oil fusing of printed wiring boards. Process control concerns, process variables and parameters for the experiment were developed.

A sample multi-layer PWB with an internal ground plane representative of a typical productio PWB was designed and fabricated. The sample PWB included plated through holes with three annular ring sizes.

Process Description

The hot oil fusing process is used to reflow/fuse the as deposited tin lead plating on PWB plated through holes. The process involves cleaning and fluxing of the PWB followd by immersion in a hot oil preheat bath, hot oil reflow bath and hot oil cool down bath. The PWB's are subsequently cleaned using DI water and forced hot air dried. A process flow chart is shown in Figure 7.

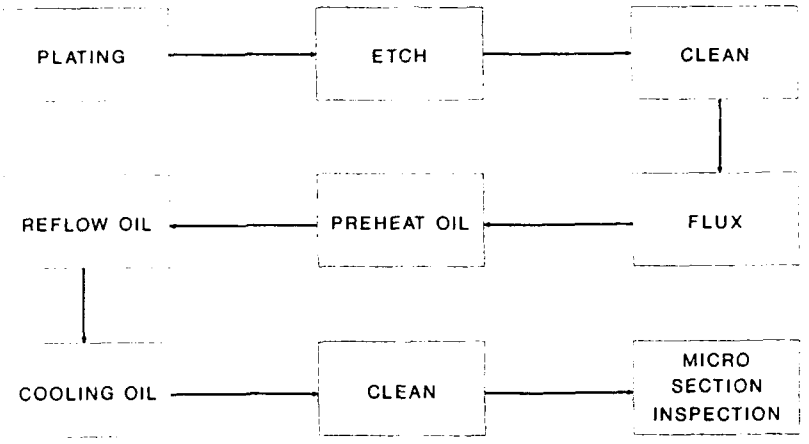


FIGURE 7. Hot Oil Fusing Process Flow Chart

Controllable and Noise Factors

The controllable factors are shown in Table 5 as six inside factors in a modified L18 orthogonal array.

The noise factors consisted of two outer factor columns to evaluate flux and oil of varying age.

TABLE 5. Orthogonal Array

L-18 ARRAY

	TIME FROM HOT OIL TO RISING	FLUX DENSITY	REFLOW TIME	ANNULAR RING SIZE	PREHEAT TIME	PREHEAT TEMPERATURE	(not used)			NEW FLUX, NEW OIL	OLD FLUX, OLD OIL
										OUTER FACTOR COLUMNS (NOISE)	
FACTOR / ASSIGNMENT	E	C	A	D	F	G	/	/			
	1	2	3	4	5	6	7	8		F1	F2
1	1	1	1	1	1	1	1	1	EXPERIMENT 'DATA CELL' NUMBER	1	2
2	1	1	2	2	2	2	2	2		3	4
3	1	1	3	3	3	3	3	3		5	6
4	1	2	1	1	2	2	3	3		7	8
5	1	2	2	2	3	3	1	1		9	10
6	1	2	3	3	1	1	2	2		11	12
7	1	3	1	2	1	3	2	3		13	14
8	1	3	2	3	2	1	3	1		15	16
9	1	3	3	1	3	2	1	2		17	18
10	2	1	1	3	3	2	2	1		19	20
11	2	1	2	1	1	3	3	2		21	22
12	2	1	3	2	2	1	1	3		23	24
13	2	2	1	2	3	1	3	2		25	26
14	2	2	2	3	1	2	1	3		27	28
15	2	2	3	1	2	3	2	1		29	30
16	2	3	1	3	2	3	1	2		31	32
17	2	3	2	1	3	1	2	3		33	34
18	2	3	3	2	1	2	3	1		35	36

Quality Characteristic

The quality characteristic for the experiment was identified as the tin lead plating thickness after fusing as measured at the crest on the pads of the plated through hole.

Five plated through holes were cross sectioned and measured on each experimental PWB following hot oil fusing.

EXPERIMENTAL RESULTS

The Taguchi Experiment on the hot oil fusing process was conducted on September 11, 12, 1991.

An Anova Table was generated using raw experimental data (plating thickness on plated through hole pads) as shown in Table 6.

TABLE 6. Anova Table

Source	Pool	Df	S	V	F	S'	rho%
E	[N]	1	146306.25	146306.25	3.33914	102490.74	2.16
C	[Y]	2	119387.17	59693.585			
A	[Y]	2	99183.167	49591.583			
D	[N]	2	2988541.5	1494270.7	34.10369	2900910.5	61.15
F	[Y]	2	118297.17	59148.585			
G	[Y]	2	5178.5000	2589.2500			
ER	[Y]	2	286670.17	143335.08			
ERR	[Y]	2	17486.167	8743.0835			
Z	[N]	1	250500.25	250500.25	5.71716	206684.74	4.36
ExC	[Y]	2	18618.167	9309.0835			
e1	[Y]	17	693460.24	40791.779			
e2	[Y]	0	0.00000				
(e)		31	1358280.8	43815.510		1533542.8	32.33
Total (Raw)	[-]	35	4743628.7	135532.25			

Level averages were then calculated. Response graphs were printed for all factors as shown in Figures 8 and 9.

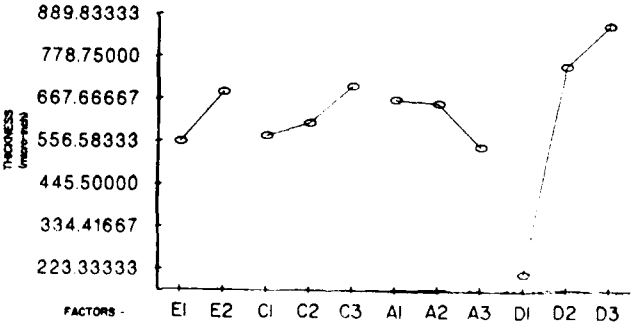


FIGURE 8. Response Graph

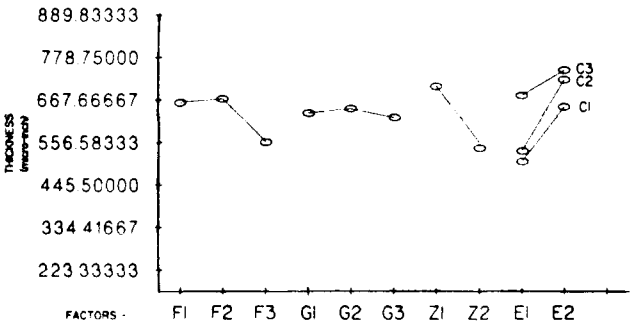


FIGURE 9. Response Graph

The level average table and response graphs were reviewed to select the optimal levels for all factors as shown in Table 7.

TABLE 7. Selection of Optimal Levels

FACTOR		OPTIMAL LEVEL	
A	REFLOW TIME	A1	BREAK
C	FLUX DENSITY	C3	960 GM/CC
D	ANNULAR RING SIZE	D3	.015 IN.
F	TIME FROM ETCH TO FUSING	E2	THREE DAYS
F	PREHEAT TIME	F2	30 SECONDS
G	PREHEAT TEMPERATURE	G2	330° F
Z	FLUX AND OIL (AGE)	Z1	NEW FLUX, NEW OIL

Process Estimate

Process estimates and confidence intervals were calculated based on the experimental plating thickness data.

Current Operating Levels
801 ± 257 microinches tin lead thickness on pad

From 594 microinches to 1058 microinches

Optimum Operating Levels
1224 ± 257 microinches tin lead thickness on pad

From 967 microinches to 1481 microinches

Potential Estimated Improvement 423 microinches

From previous investigation, the desired range of plating thickness after fusing for improved solderability and robustness against aging was determined to be 700 microinches to 1000 microinches minimum.

As shown by the process estimates, the suplier potentially had the process capability to achieve the 700 to 1000 microinch goal using the optimum levels identified by the experiment.

CONFIRMATION EXPERIMENT

A confirmation experiment was conducted on October 30, 1991. Twelve PWB panels designed for the original hot oil fusing experiment were hot oil fused using the optimum levels for the six controllable factors. The fusing oil was one day old when the confirmation experiment was conducted. Following the hot oil fusing, the PWB's were sectioned and five plated through holes were measured for tin lead plating thickness at the crest on the pads. The summary of the confirmation experiment is shown below:

Optimal Process Estimate Average	Confirmation Experiment Results
1224 microinches (optimal)	904 microinches
1057 microinches (optimal except Z2, old oil)	

Although new oil contributres to optimal results, it becomes economically impractical to constantly maintain "new" oil. The appearance of the oil from one to three days use was not observed to vary appreciably. One week "old" oil as used in the original experiment exhibits a significantly darker color and accumulation of flux and other contaminants. The oil was changed by the supplier at least once a week. This practice was to continue by the supplier with further evaluation to be conducted by the supplier of the time and surface area processed between oil changes.

The confirmation experiment verified the supplier's process was capable of yielding the desired plating thickness of a minimum of 700 to 1000 microinches after fusing.

IMPROVEMENTS DEFINED

Implementation of the optimum levels for the hot oil fusing process resulted in an average incrase of 13% in tin lead plating thickness after fusing.

Variability of tin lead plating thickness after fusing was reduced from a range of 800 microinches to 500 microinches after implementing optimum levels.

Significant process factors affecting the results of the hot oil fusing process were identified and controlled.

The capability of the supplier's hot oil fusing process was determined.

CONCLUSION

IMPROVEMENT SUMMARY

Figure 10 illustrates the wavesolder defect trend for a seventeen week period (beginning at the Work Week 14 high point of 6800 PPM) during which time process improvements were made. Work Week 15 to 17 reductions are attributed to the segregation of very old (1+ year old) PWB's with supplier fabrication anomalies and the implementation of optimum settings from the wavesolder experiment. During Work Week 18, 150 rejuvenated and 250 new (thicker plating) PWB's were wavesoldered. Work Weeks 18 to 21 represent the availability of new, thicker plating PWB's. Work Weeks 22 and 23 indicate anomalies with the thicker plating supplier process. The supplier provided initial corrective action Work Week 27. Rejuvenation of PWB's for production began approximately Work Week 25. The thicker plating supplier quality remained steady during Work Weeks 27 through 31, but required improvements. A/CD Rockledge Manufacturing Engineering visited the supplier and began planning an experiment Work Week 31 for the supplier's hot oil reflow process. A successful experiment was conducted in September, 1991, during Work Week 37. A confirmation experiment was conducted in October during Work Week 44. PWB's fabricated Work Week 44 and wavesoldered by A/CD Rockledge Work Week 46 indicated an improvement in solderability.

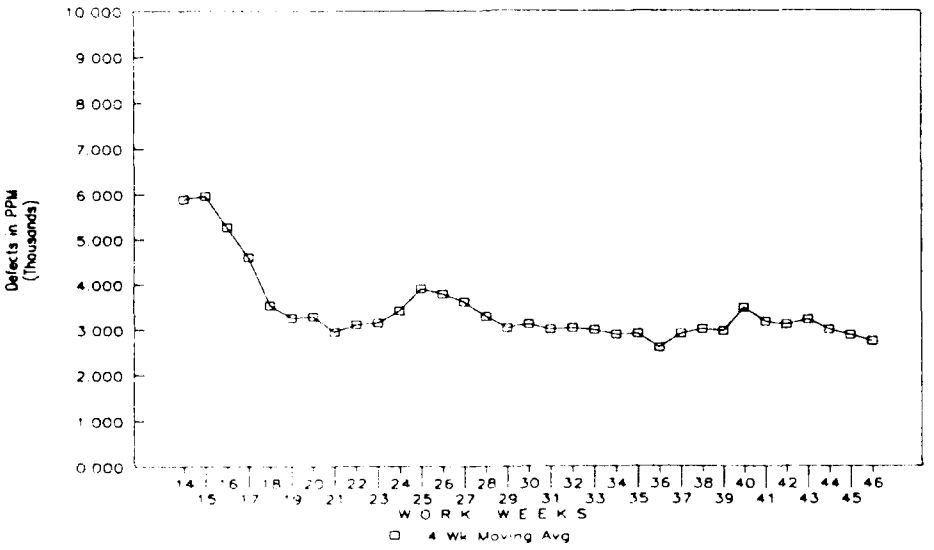


FIGURE 10. Wavesolder Process Yield

COST SAVINGS

Cost savings were estimated for the initial wavesolder process experiment and cost avoidance and potential cost savings were estmated as a result of further investigation of the supplier's process.

Cost savings, shown in Table 8, were based on actual production data (rather than the optimum setting process estimate) due to the variability of the process with old PWB date codes.

TABLE 8. Cost Savings

Wavesolder Process Experiment	
Experiment Cost	
Operators	26 hours
Engineering	96 hours
Estimated Savings	
Reduction of wavesolder defects (1353 PPM) per CCA	$ 56,816
Further Investigation (Including Supplier Process)	
Further Investigation Cost (through Work Week 44)	
Operators	34 hours
Engineering (including report)	680 hours
Other Operations Support Personnel	306 hours
Further Investigation Savings	
Non-Recurring (rejuvenated PWB material)	$288,700
Recurring wavesolder defect Reduction (based on current level of 2500 PPM)	$180,600
Recurring non-conforming material disposition	$129,525
Total Recurring Annual Savings	$310,125

Future efforts to reduce the wavesolder defect rate by eliminating old boards, phasing out the need for rejuvenated PWB's and procuring high quality new PWB's may result in further cost savings. As shown earlier in the report, defect rates as low as 837 PPM were attained for new, thicker plating PWB's.

DID RESULTS MEET OBJECTIVES

Results of the initial experiment and further nvestigation did meet the objective and goals for the following reasons:

- The number of wavesolder defects per Circuit Card Assembly were reduced from 6800 PPM to a current level (Work Week 46) of 2200 PPM. Further improvement is anticipated.

- Best wavesolder process settings were derived from the wavesolder process Taguchi experiment.

- A better understanding of ITT A/CD Rockledge PWB solderability requirements by the PWB suppliers and Rockledge Operations was established by implementing an A/CD Rockledge PWB Solderability Requirements Specification in the MRP system as a purchase order requirement for all programs at A/CD Rockledge.

- As a result of the PWB specification, an awareness has been established concerning the importance of procuring and using PWB's in a timely manner at A/CD Rockledge.

- A joint effort was established between ITT A/CD and PWB supplier to conduct a Taguchi experiment to evaluate the hot oil fusing process and to implement statistical process control. Consistently thicker plating was evident on production PWB's fabricated after the experiment improving PWB solderability.

In accordance with the initial objective of the investigation, A/CD Rockledge will continue to be attentive to in-house process controls and collaborate with printed wiring board suppliers in an effort to seek continuous process improvement.

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Reliability of Surface-Mount Electronics Assemblies Cleaned Using CFC-113-free Techniques

by

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ABSTRACT

This paper summarises briefly all the substitutive techniques for CFC-113 and 1,1,1-trichloroethane blend cleaning, including the use of "no-clean" and controlled atmosphere soldering but with emphasis on high-reliability applications. Each technique is evoked on the influence it can have on the final reliability of the assembly under normal and abnormal storage and working conditions. Reliability, generally, is determined by numerous other parameters which are frequently ignored, such as the component layout for best cleaning quality. The requirements of conformal coating are also frequently skimped over. In practical terms, this paper may help those selecting a substitutive soldering/cleaning process to choose one which will meet their quality requirements at minimum costs.

INTRODUCTION

Up to recently, little thought has been applied to the reliability problems engendered by the presence of contamination on electronics assemblies or its corollary, cleaning [Reference 1]. Two military specifications [Reference 2, 3] pioneered the notion of checking for certain contaminant species in the USA and the UK, but little research has been done to correlate the causes and the effects on the reliability of the finished products, or even to determine the acceptable quantities of residual contamination under any given set of conditions. An important research project has been started by the Swiss Federal Institute of Technology, Zurich to examine the overall aspects of Reliability and SM Technology, under the authority of Professor A. Birolini, Chair of Reliability [Reference 4]. Cleaning is one part of this project, in which a provisional working matrix is currently in the course of elaboration. This will involve at least:

- solder pastes with at least four different chemistries
- reflow and wave soldering
- "no-clean" and five different cleaning techniques
- layout design factors.

The output parameters are, for the moment, less well defined but will probably include:

- Ionic Contamination Testing
- SIR testing under steady 35–40°C/95% RH conditions
- SIR testing under steady 85°C/85% RH conditions
- Vesication testing with a single thin conformal coating
- SIR testing under different test and bias voltage conditions.

It is not envisaged that dynamic electronic functional reliability be determined at this stage as a function of the soldering/cleaning conditions. This is because funding is limited and the cost of determining whether each failure under dynamic conditions is a function of soldering/cleaning or because of extrinsic factors would become astronomical. Nevertheless, if funds to do this became available, the project could be expanded. This would then become the first academic work that could correlate contamination and surface insulation resistance values to different failure mechanisms. It is without doubt that this would have an enormous practical importance as it is almost universally agreed that, whereas we have an empirical idea of acceptable contamination levels for given applications, we do not *know* what scientifically-proven correlations exist between contamination types and levels and failure mechanisms and, hence, reliability. We therefore base much of our decision-

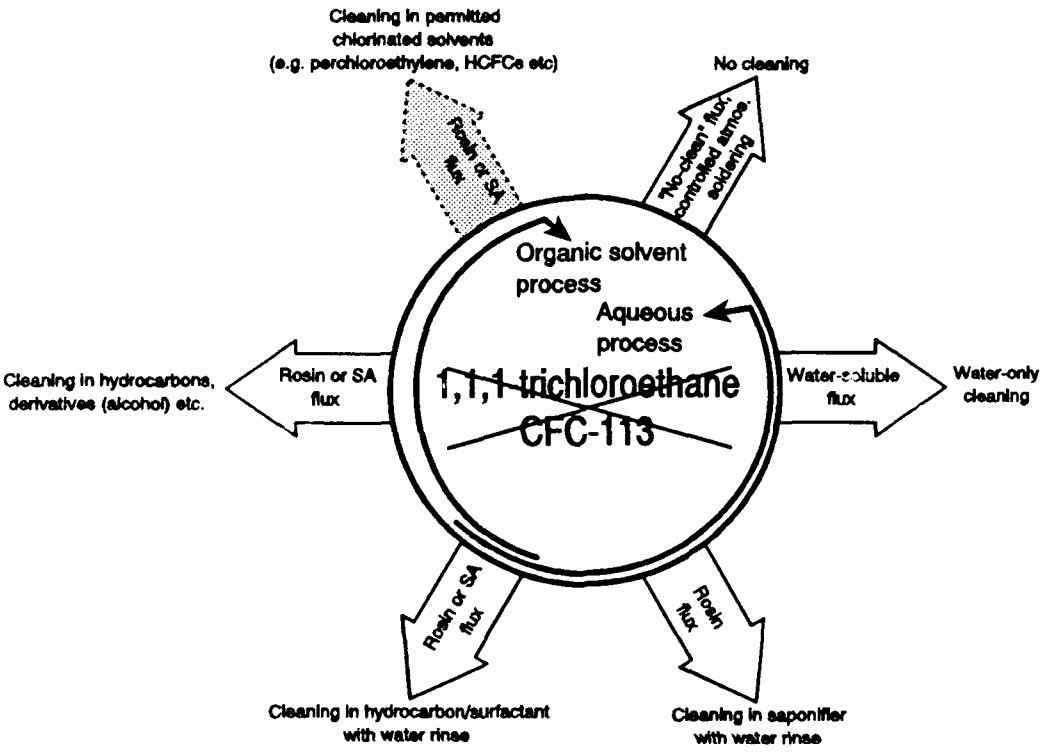

FIGURE 1. Schematic of Substitution for O.D. Solvents

making in this field on conjecture. Unfortunately, such funding could not come from academia and industry has not been able to be too generous over the past year or two, despite the fact that they are the most likely to benefit from such research.

The situation regarding the correlation of cleaning and reliability has recently changed because of two important factors. The first is the discovery that the habitual cleaning solvents, based on CFC-113 and 1,1,1-trichloroethane, were partially responsible for stratospheric ozone depletion. The other is the widespread introduction of surface mount techniques which are somewhat contradictory to good surface cleanliness, hence reliability.

THE MONTREAL PROTOCOL

The Montreal Protocol is an international agreement limiting, and finally forbidding, the use of most ozone depleting substances. It was signed in September 1987 and the first amendment was signed in June 1990. A second amendment will be signed in October 1991. The 1990 amendment was deliberately severe as research since 1987 had shown that the initial measures were insufficient to preserve the stratospheric ozone in quantities ample enough to prevent excessive solar radiation from reaching the biosphere. As the situation has now been shown to be even worse than was thought then, it is no secret that the 1991 amendment will probably be even more severe, to the extent that world industry will be hard put to conform to the probable measures. Early indications (late September 1991) show that the Antarctic "ozone-hole" is starting to be measurable at least one to two weeks earlier than has been possible in past years, but this may also be partially due to more sophisticated instrumentation. A recent news report [Reference 5] indicates a possibility that inhabitants of Tierra del Fuego and Southern Patagonia are suffering from an increase of ultra-violet light-related ocular diseases, ascribed to ozone depletion.

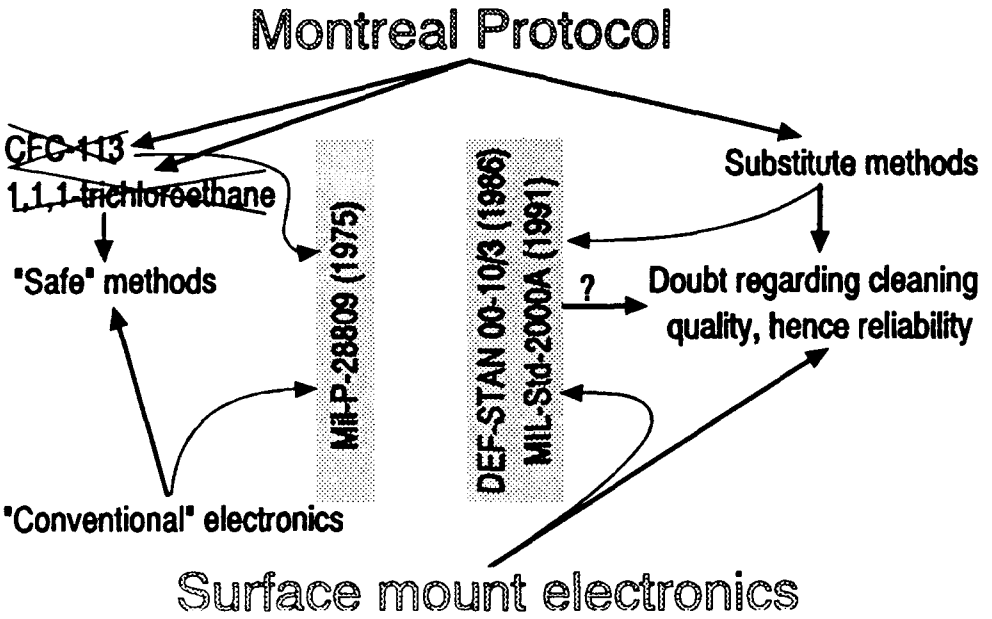

FIGURE 2. Evolution of Reliability and Cleaning

The cleaning solvents most affected by the Protocol are 1,1,2-trichloro-1,2,2-trifluoroethane (CFC-113) and 1,1,1-trichloroethane (also known as methyl chloroform). Both of these are used, amongst other applications, for removing flux residues from soldered printed circuit boards. They are generally sold under a number of trade names. In Switzerland, Germany and some other "head-start" countries, legislation has been passed that will forbid their use as early as the end of 1992 (Sweden since 1 January 1991). In most of these countries, it is very unlikely that any derogations will be allowed for defluxing assemblies.

This situation has forced industry to seek rapidly other means of cleaning electronics assemblies or even to abandon cleaning [References 6, 7]. The implications of this sudden change in techniques, in terms of assembly reliability, are not fully known, but neither is a truly dependable yardstick against which to measure the effects of these sudden changes of thought.

Six substitution methods (Figure 1) are commonly being applied to move away from the traditional rosin flux soldering and CFC-113 azeotrope or 1,1,1-trichloroethane cleaning. It is almost indisputable to say that this is causing a revolution in the industry. The traditional method has been "comfortable" because any errors in the cleaning process did not necessarily produce catastrophically poor results and many users firmly believed in the "slosh it around in a bucket of solvent and it was clean" approach. Quite apart from the poor science in this approach, it engendered a false sense of security (Figure 2). Since research started on substitute processes, it has been shown that this traditional way was much worse and much more expensive than some others which were decried in the past (Table 1). The first winds of change blew with the publication of the UK DEF-STAN 00-10/3 in 1986 which encouraged the use of aqueous methods, whilst not forbidding the use of halocarbon solvents. This standard was the result of several years' R&D work by the Ministry of Defence who showed unequivocally that the use of many water-soluble fluxes did not produce any deleterious effects on the reliability of the assemblies.

THE EFFECT OF SURFACE MOUNTING

Surface Mount Techniques (SMT) introduced some new parameters into the reliability equation. Some of these, such as the differential expansions of components and substrates, have been the subject of much literature.

TABLE 1. Résumé of Characteristics of Major Processes.

	Cleaning machinery	Cleaning process	Overall cost	Energy requirements	Environmental/ safety hazards	Military usage	Cleanliness/ Reliability[a]
"No-clean" technique	NA	NA	Low	NA	NA	Theoretically possible but unlikely in practice	Mediocre to good
W/S flux + water	Simple, medium cost	Simple, very low cost	Average	Average	Very low, water treatment	Used and approved in several locations	Average to excellent
RA + saponifier + water	Simple, medium cost	Simple, low cost	Average to high	Average	Low, water treatment, slightly toxic	Used and approved in several locations	Average to very good
RA + HCS + water	Complex, high cost	Complex, very high cost	Very high	Very high	Medium, water treatment, slightly toxic, VOCs	Used and approved in several locations	Average to excellent
RA + alcohol	Complex, very high cost	Complex, very high cost	Very high	High	High, explosive	Theoretically possible but no usage known	Poor to good
RA + low-volatile HC derivative	Medium, medium cost	Medium, medium cost	Average to high	Medium to high	Low, air treatment	Too new for acceptance trials: probably OK	Too new to be known, probably average to good
RA + halocarbons	Simple, low cost	Complex, average cost	Average	Low	Very high, toxic, VOC, global warming	Used and approved in several locations	Poor to good

[a] using best available machinery and techniques under production conditions.

Defluxing has been another such controversial subject. Generally speaking, three schools of thought have predominated the published information. These have all a certain element of verity but none of them even approach the whole truth. They are:

1. the conservative school: only current methods using solvents containing ozone-depleting substances can ensure adequate cleanliness. As much as anything, this school reflects either ignorance or the inability to face change. Its main argument is based on the belief that aqueous or other cleaning methods cannot penetrate freely under SM components where the spacings between them and the substrate are often less than 0.1 mm or that drying was too energy-consuming. These arguments are fallacious. A secondary argument, even more fallacious, is that many electronics components are incompatible with any cleaning solvent or solution other than CFC-113. This may have been true forty years ago but, today, there are components of all types available that will support any cleaning method.
2. the eco-"non-clean" school: only by not cleaning can economical and ecological sense prevail. In a certain measure, this must be intuitively true, but the question whether sufficient reliability for the application will result must be very seriously considered. This is the obvious choice for any application where reliability is a relatively secondary consideration (e.g. consumer goods, telephones, low-cost office equipment, personal

computers etc.). It is probable that "no-clean" fluxes would be sufficiently good for at least half of the world electronics production.

3. the modern school: only by cleaning using the latest methods can reliability be achieved, no matter what the cost to the economy or to protect the environment.

To illustrate these schools of thought, let us look at the automotive industry which, itself, is being revolutionised by the introduction of electronics increasingly into ordinary passenger cars. There are three types of electronics in modern cars: car radios for entertainment, CD and tape players; non-essential functional electronics (e.g. central locking, window winders, telecommunications etc.); and essential functional electronics (e.g. engine controls and braking systems etc.). If the first category fails, no harm to the occupants could possibly arise. In the case of a failure of the second type, it may be niggling or frankly inconvenient, but not dangerous (a failed opening roof winder control may cause rain to be let in but the roof can be closed mechanically after a couple of minutes with a screwdriver). However, failure of the third class may be fatal for the driver.

This author has recently discussed this problem, at length, with representatives of four companies manufacturing automotive electronics. Two of them approached the subject with the view that the most important aspect was the lowest economical production costs. In one case, they soldered using conventional wave-soldering techniques with a low-solids "no-clean" flux without any cleaning. To mitigate the lowered reliability, the units concerned were placed in the passenger, rather than the engine, compartment. However, everyone knows that the inside of a car can range from very, very cold to very, very hot and from dry to condensing. The question must seriously be asked whether this manufacturer has done his homework correctly, knowing that the flux he has selected is amongst the most aggressive and corrosive of such types. (Another manufacturer has been reported to have followed this same line in recent months, but he carefully tested several fluxes before choosing one which is probably amongst the least aggressive.)

The second manufacturer also used no-clean soldering, this time with a controlled atmosphere soldering machine. The quantities of residue are significantly lower and a conformal coating is applied on top of the uncleaned boards. This type of manufacture will probably produce more reliable results than the last one, but there is more than a niggling doubt left in one's mind about the wisdom of encapsulating metallic salts and organic acid residues under a conformal coating, especially in view of the extreme conditions cars must operate in.

The third manufacturer viewed cleaning as essential for reliability and did not change his soldering process. Cleaning is done by saponification using top-quality high-throughput batch machines, followed by sampling ionic contamination controls. This view is serious and the standards applied are slightly more severe than are required for military electronics. From the point of view of assembly reliability (discounting component reliability), this would seem a good solution.

The last manufacturer, a Japanese one, is approaching the subject even more seriously. For some applications, they have already converted to water-soluble soldering techniques, with adequate controls. For others, where water-soluble flux may cause other problems, a large research programme has been established. When visiting this factory, this author was impressed by the serious approach and when commenting on this, the following anecdote was told: a motorist (with a car made elsewhere than in Japan) in the wilds of Northern Canada had an engine failure due to faulty electronics in winter. He perished of exposure to the cold, as there was no traffic at that particular location. Quite apart from the legal liability aspect of this kind of matter, this company felt they had a moral responsibility to ensure that their products were as reliable as was humanly possible. In aircraft, essential electronics were frequently doubled or tripled up, but not in cars. Where redundant electronics [Reference 1] are not applied, then reliability must be at least as good as for military electronics, if not better in view of the harsher operating conditions. It would possibly be even better if completely independent and dissimilar redundant systems were applied in cars with warning lights if any redundant part failed. In this way, it may be possible to reduce the inherent reliability by less-than-perfect cleaning, even if the performance of the secondary system was reduced. This is perhaps analogous to the "limited-performance" spare wheel—sufficient to get you home without the expense, weight or volume of a full exchange wheel/tyre assembly.

While on this subject, an interesting table has been published [Reference 8] showing the environmental hazards of nine typical use categories. Other than the fact that it shows that the "Automotive-under-hood" category is subject to the worst T_{min} and T_{max} values, it also has the widest ΔT_{max} in the shortest $t_{\Delta T}$ with one of the largest number of cycles per year. An automobilists' association has recently published [Reference 9] a statistical survey of some 200,000 breakdowns that occurred on Swiss roads in 1990 to which it intervened. One table showed the causes of such breakdowns against models. It is perhaps significant that, with only one exception, all listed makes of European cars (including luxury ones) had significantly high rates of engine electronics failures, in some cases the most frequent cause of "walk-home" breakdowns. With no exception whatsoever, no Japanese model was cited as having any engine electronics failures. Whereas there is absolutely no proof that this situation is related to cleanliness, it may be conjectured as one possibility, knowing that Japanese manufacturers are much more conscious of the importance of cleaning for reliability than some of the European or American ones and also knowing that some of the Japanese designs are, in fact, European, manufactured under licence.

CLEANING METHODS

There is a considerable choice of cleaning methods, as summarised in Table 1. Each has its advantages and its disadvantages but all are possibilities — sometimes at a price — for high-reliability electronics. As this paper is concerned principally with electronics for military, aerospace or similar applications, and as "no-clean" fluxes have not yet been considered as suitable for these, this technique will be ignored here.

WATER-SOLUBLE FLUXES + WATER WASH

More ink (and not always water-soluble ink!) has flowed on this subject than on other cleaning methods. It is a passionate debate which leaves no-one indifferent: either one is strongly for or one is strongly against, with very few persons adopting a middle line. Because it is so passionate, there have been quite a lot of arguments, both pro and con, put forward that have been exaggerated, to the point of extremism on occasion.

Dispassionately, it can be said that this method can give excellent results if it is treated with respect. One of its major virtues is the fact that we have an excellent track record of its use in large quantities for soldering PCB assemblies over more than 25 years. Many of the companies who have used it consistently, such as most of the large computer and instrumentation manufacturers, have developed a reputation for quality products.

There is one proviso to its use for high-reliability applications: if you do not possess the equipment with excellent process control that can ensure an adequate cleaning quality and if you do not possess the means to statistically analyse the results, then forget this method. It is not for dilettantes or amateurs. On the other hand, if you approach it in a fully professional manner, it can not only produce amongst the best results, it is surely the cheapest of the cleaning methods.

Its main counter-argument is that it is claimed to cause significant reductions in the Surface Insulation Resistance. This is very much dependent on the composition of the flux: many will hardly lower the SIR whereas others may drop it by two orders of magnitude. There would seem to be two distinct phenomena which can cause the effect. The more usual one is that the flux vehicle is in the form of linear micelle-forming liquid polymers. These have their hydrophobic ends with a strong affinity to the organic substrates and the wash energy is insufficient to break the Van der Waals bonds. The other ends have an -OH radical which renders the surface slightly hygroscopic and the absorbed moisture causes the SIR drop. As such, this is not catastrophic, as the vapour pressure of these substances can rise to quite high levels at elevated temperatures or even at room temperature. In time, these substances can simply evaporate from the surface and the SIR rises again. This phenomenon is not unique to water-soluble fluxes as some rosin or resin fluxes may contain similar chemicals and others may contain carboxylic acid activators which may behave in a similar way. The drop of SIR from this cause is usually insufficient to compromise the reliability, assuming a good cleaning operation.

The other phenomenon is similar except that it is aggravated by the substrate being physically attacked by the same substances. This can happen if the laminate or the solder mask (resist) has not been fully cured. Where the cross-linking is incomplete, the partial polymers are actually removed from the PCB by the micellar action

of these molecules. As this occurs round the boundaries of well-polymerised molecules, it is rather akin to a crazy paving with deep cracks between the stones. The micelles enter the cracks *allegro vivace* and tend to stay there for ever. Because of the physical constraints within these molecular cracks, evaporation is almost impossible, so that the SIR from this cause will not rise again, or very little so. This is therefore a much more serious phenomenon which can compromise long-term reliability. The remedy is simple: use only top-grade materials which are formulated and mixed to ensure as complete a cure as possible of the laminate and the solder mask — and test the cure. The drop in SIR with this phenomenon is often sufficient to cause concern for high-reliability applications, even though little documentation appears to be forthcoming that proves the reliability to be really compromised for most circuitry. Prudence may therefore be called for.

Solubilisation of all the soldering residues is generally excellent with both liquid fluxes and pastes. Pastes have some particularities in practical terms. They contain considerable quantities of agents designed to adjust the viscosity/thixotropy, the tackiness and slumping. In addition, they often contain some surfactants or other additives to ensure the solubilisation of all the other chemicals. This makes what may almost be described as a post-reflow witches' brew which, although perfectly water soluble, may cause problems in the cleaning machine if allowed to become too concentrated in the wash water. As a general rule, it is necessary to have a greater throughput of water when using pastes than with liquid fluxes. Cases of redeposition of noxious compounds on circuits, although rare, have been known to occur and would certainly cause a drop in reliability figures.

ROSIN FLUXES + SAPONIFIER + WATER WASH

Saponifying rosin fluxes is another method with a good track record over twenty-plus years. It has almost exactly the same advantages and disadvantages as the previous category, plus a few of its own. Its major advantage is that it can be configured for almost any rosin flux, be it R, RA, RMA, RSA, organic-acid activated and even low-solids types, with good results in all cases (perhaps after juggling with the saponifier type, concentration, wash time and temperature). This means that, in most cases, it is quite unnecessary to change one of the more important parameters that the users are comfortable with, namely the flux type and, consequently, the machine settings. It is important to understand that saponification is not an instantaneous process whereby all the rosin is solubilised in a flash. It is more like onion-peeling, whereby one removes a thin layer at a time, while exposing the next one. On thick rosin deposits, this may take up to two minutes or even more if they are under SM components. It is therefore useless to expect good solubilisation of the rosin if the saponifier solution is not sprayed energetically onto the parts being cleaned for a good length of time. This rules out short conveyorised machines with fast conveyor speeds. Before adopting this process for high-reliability electronics, make sure of this point. Ideally, as with all high-reliability work, top quality automatic batch machines (such as of the high-throughput type) will give consistently better results than either small batch machines or most conveyorised ones, because of their flexibility.

The overall reliability of circuits optimally cleaned using this process is usually more than enough for even stringent military applications, although marginally more contaminated than with water-soluble fluxes. Again, a fully professional approach is required to achieve this level of reliability. Overall cost is slightly higher than the last category.

ROSIN FLUXES + HYDROCARBON/SURFACTANT + WATER CLEANING

Hydrocarbon/surfactant (HCS) cleaning, sometimes incorrectly, vaguely and misleadingly referred to as "semi-aqueous" cleaning, is the new boy in the regiment of aqueous cleaners. It is an aqueous cleaning of the residues from a solvent process, the latter initially solubilising the rosin. Although more popular over the last five years, this method has two outstanding characteristics: it is effective and expensive. Its efficiency leaves little doubt: properly used, it will produce the cleanest circuits of any method and the short field record available has demonstrated a good inherent reliability. It is expensive because the products are not cheap to buy and the machines generally require a high capital investment of the order of 50—100% higher than for the previous processes. Typical overall costs may be at least twice those of either of the foregoing methods, sometimes considerably more.

ROSIN FLUXES + HYDROCARBON DERIVATIVE CLEANING

This category may be divided into two sub-categories, each of which requires a separate discussion. They have in common the fact that the rosin and other contaminants are removed in successively cleaner solvent baths or sprays, the last treatment being with continuously repurified solvent. From there on, the resemblance ends.

Light HC Derivative Cleaning

As a general rule, the solvent used for this is a light alcohol, blended or pure. Isopropanol is frequently a good compromise between cost, toxicity and cleaning efficiency. This process caused a sudden surge of interest in Europe two years ago but it has since succumbed almost into oblivion. This is because of a combination of three factors:

- The flammability or explosibility required massive and expensive measures to ensure sufficient operator safety
- The solubility of some of the post-soldering metallic salts is very small
- The energy consumption for the distillation is very high.

That having been said, a variation on this theme has appeared on the scene, alcohol cleaning using a perfluorinated ether vapour phase blanket in a "tight" machine. Still somewhat in its infancy, accurate figures regarding costs and the reliability of cleaned boards have yet to be published.

Heavy HC Derivative Cleaning

This process employs pure or blended heavy alcohols, ethers or esters or similar oxygenated hydrocarbons. It is fairly new and reliable information is extremely difficult to obtain. Different products are being proposed with closed cup flash points within the range of 45—110°C and boiling points in the range of 100—220°C. One of the difficulties with this method is to repurify the final rinse solvent. Carbon filtration plus deionisation has been proposed but has not been conclusively proven as at the time of writing. Another problem is that drying demands hot air blasts and is relatively slow. Being a new process, no practical field trials data is available. *A priori*, it is probable that the cleaning quality will be adequate for high-reliability work, but may not be quite as good as some of the other methods. Cost is likely to be intermediate between HCS cleaning and that of other aqueous methods.

"PERMITTED" HALOCARBON CLEANING

The crux of this discussion is what is claimed to be permitted. Heavily ozone-depleting solvents are clearly not. PAFTI to III tested HCFCs are either too ozone-depleting or too toxic. PAFTIV testing of HCFC-225 isomers will not be completed before about 1995. Perchloroethylene and trichloroethylene are regarded with suspicion in the electronics industry, as being rather too aggressive and too toxic for ease of use. This leaves very little and, for this reason, it is not proposed to expand this theme.

FAILURE MECHANISMS

There are several failure mechanisms [References 10, 11] resulting from contamination which may seriously reduce the reliability of surface mount assemblies. The causes can be broadly classed as:

1. pre-soldering contamination
2. post-soldering contamination
3. handling contamination
4. cleaning problems
5. conformal coating problems.

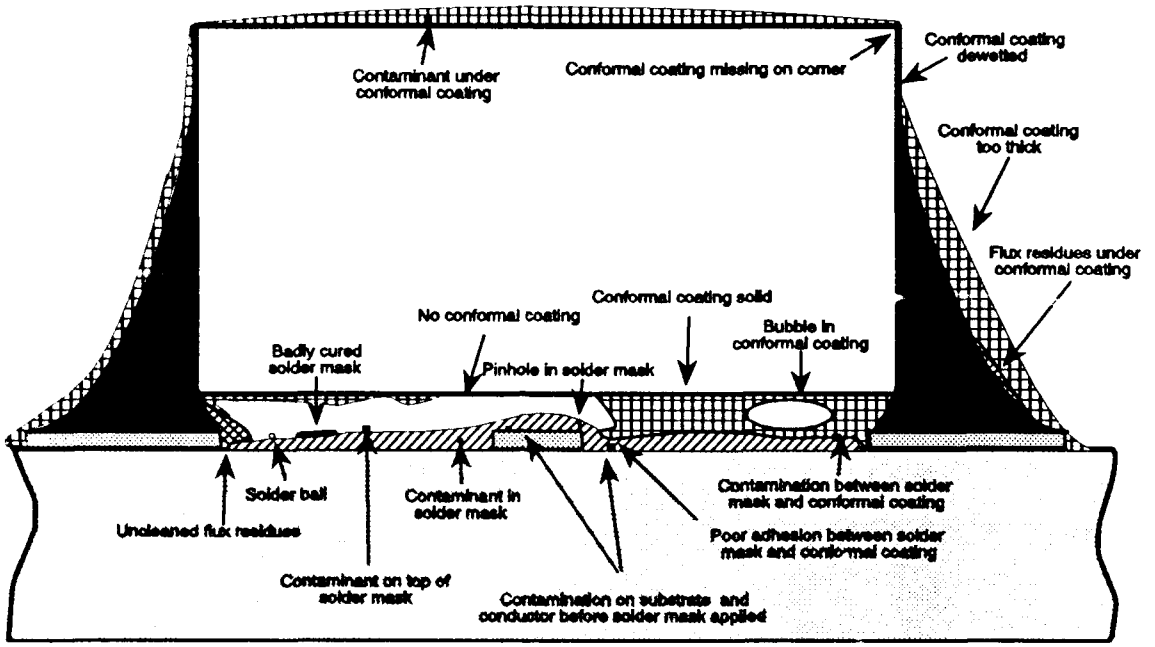

FIGURE 3. Schematic of some Contamination-related Faults.

Figure 3 is a graphic representation summarising many of the main problems. The above-listed causes will be examined in turn and each one will be discussed briefly, both in terms of prevention as well as cure, where such is applicable.

PRE-SOLDERING CONTAMINATION

The origins of this class are wide and varied. If cleaning is subsequently carried out, then the effects may be mitigated, but rarely eliminated. Where subsequent cleaning is not carried out, then this type of contamination may be the cause of very severe reductions of reliability.

The main origins are the contamination of the bare printed board itself, the components mounted on it or handling contamination during the assembly process. As far as the board itself is concerned, other than handling contamination, the most important contaminants are residues from fluxes and other chemicals employed in the printed circuit manufacture, poorly polymerised or chemically attacked substrate material, absorbed or adsorbed chemicals, solder masking over contaminants, poor quality solder masks etc.

Components vary enormously from very clean down to abominably contaminated. This author recently asked an audience of nearly 100 engineers concerned with reliability for a show of hands of those whose organisations tested incoming components for contamination: the response was zero. Yet about 30 showed they did not clean and most of the participants indicated they were concerned about the cleanliness, as well as the reliability, of the finished assembly. This is mind-boggling.

Contaminated components very frequently solder badly, as well as cause subsequent problems. One of the major problem areas is with hot-tinned components. These are customarily tinned using active water-soluble fluxes and any post-tinning cleaning may be skimpy or even not carried out. These components pass the main tests at the factory but deteriorate rapidly thereafter. It has been known for active components to be so corroded after a few months that they were completely unsolderable. Even if they are sufficiently solderable, the same residues may create corrosion or dendrite formation at any later date.

It should not be thought that, if subsequent cleaning is carried out, this will necessarily remove all pre-soldering contamination. Many of the cleaning methods used for post-soldering flux removal are specific to the flux type used and are unspecific to other types of contaminant. Furthermore, the temperature of the soldering operation may modify the prior residues chemically by decomposition or polymerisation, rendering previously soluble contaminants completely insoluble.

One very strong word of warning is in order if no subsequent cleaning is carried out, either using the so-called "no-clean" fluxes or controlled atmosphere soldering. In both cases, the chemical composition of the residues is determinant for the reliability. For example, in the case of low-solids fluxes, the activators and their by-products are frequently held in a rosin or resin matrix. This is carefully balanced. The presence of other contaminants may upset this precarious balance, releasing aggressive substances to where they can cause the most harm. If even a moderate reliability is required, all the components, including the printed circuits, must be perfectly cleaned before assembly. This is really only displacing the problem of cleaning, not eliminating it. On the other hand, if all the components are provably clean before assembly and the assembly process does not introduce new contaminants, then not cleaning may be viable for applications requiring a reasonable reliability. Notwithstanding, for directly or indirectly life-dependent requirements, the risk incurred by adopting "no-clean" techniques may be too great, particularly if there is any chance that the assemblies will be used under poor environmental conditions.

Assembly obviously requires minimum new contaminants to be added. Common sources are lubricating oils from assembly machines, oil and water mists from pneumatic operating cylinders, poor adhesive compositions, dust, fingerprints etc.

Strictly speaking, solder pastes are applied prior to soldering, but they will be discussed in more detail in the next section.

POST-SOLDERING CONTAMINATION

The discussion in this section will be confined uniquely to flux and solder paste residues after soldering. Modifications of these because of other reasons, such as the presence of pre-soldering contamination, will not be treated.

The residues from fluxes may be characterised as containing some or all of the following:

- unmodified resin or rosin
- thermally decomposed or polymerised resins or rosin
- hydrolysed rosin
- low-volatility vehicles
- unmodified hydrohalide activators
- decomposed hydrohalides
- unmodified carboxylic acid activators
- decomposed carboxylic acid activators
- polymerised carboxylic acid activators
- metallic halides
- metallic carboxylates (including from rosin)
- solder paste modifiers
- etc.

To remove all of these is a formidable task for any cleaning process and it speaks wonders that we are able to achieve high reliability by thus cleaning. The most important components that must be removed as thoroughly as possible are all the modified and unmodified halide and carboxyl groups. As a general rule, rosin and

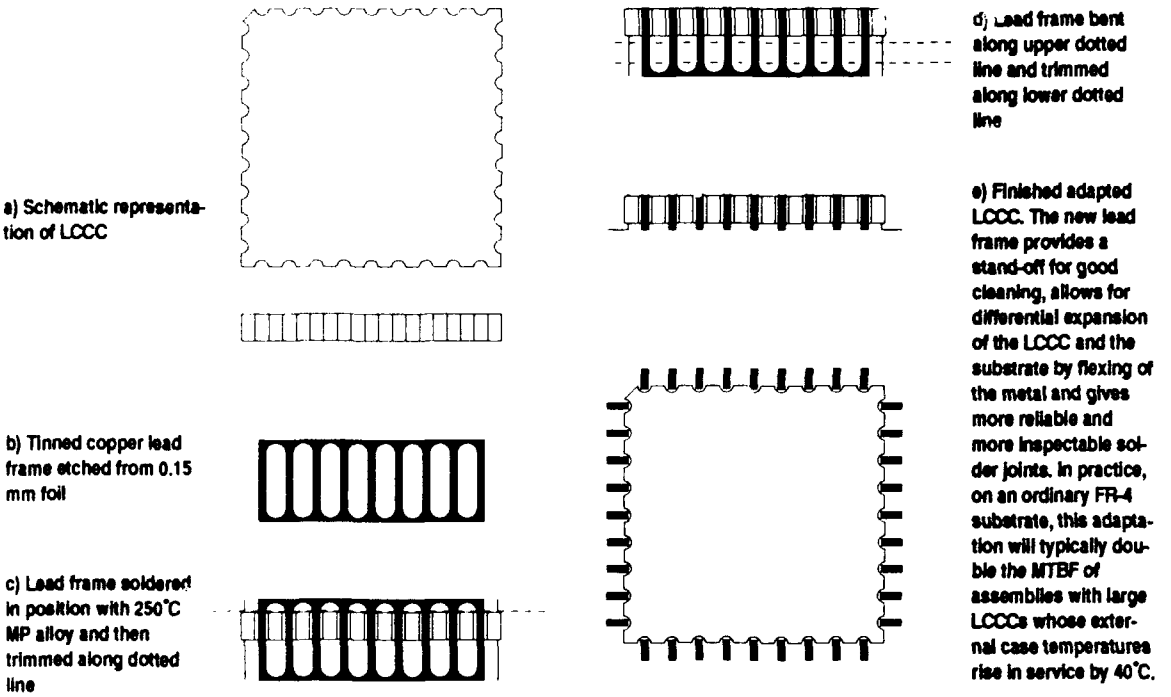

FIGURE 4. Adapting LCCCs with a Lead Frame.

resins are fairly inert and minute residual quantities may not pose a serious problem. Solder paste modifiers do sometimes represent a difficult as they may be both difficult to remove and hygroscopic. The fact that they are always concentrated round the solder joints, i.e. where they can cause the most harm, only serves to aggravate the problem. One problem that occurs with the modifiers is that they may be solubilised in the wash water by surfactants present in the paste but are then re-precipitated in the rinse stage as there may not be sufficient surfactant dragged out to be effective at the low diluted concentrations. This may be aggravated if foaming from the surfactants occurs in the wash stage as incipient precipitation can sometimes be observed actually in the foam. A small quantity of an anti-foam (not based on silicones, of course!) will usually keep this problem under control.

HANDLING CONTAMINATION

This has been evoked in the section on Pre-soldering Contamination as applied to the assembly process.

Once cleaning has been carried out, care must be taken not to re-introduce contaminants onto the assembly. This implies moderate routines to keep the assembled circuits away from any contamination source, including ungloved hands. One source that is frequently ignored is the use of certain types of anti-static materials. These may function according to several principles, e.g., plastics that are rendered mass-conductive by the addition of inert conductive material, such as carbon, plastics that are rendered surface-conductive by the surface evaporation of a metallic film and plastics that have a high proportion of hygroscopic materials incorporated whose absorption of humidity is sufficient to render it slightly conductive. Some of the latter type allow the transfer of small quantities of the hygroscopic additive by contact or by sublimation onto the assemblies packed therein. These additives are non-ionic but their hydrophilic micellar structure does not necessarily make for easy removal from electronics assemblies and they certainly would be deleterious to substrate insulating properties if they were transferred to them, hence to the reliability. Experience shows that metallic surface-coated anti-static plastic film without plasticisers is the best compromise for the immediate primary packing for electronics assemblies, in terms of contamination.

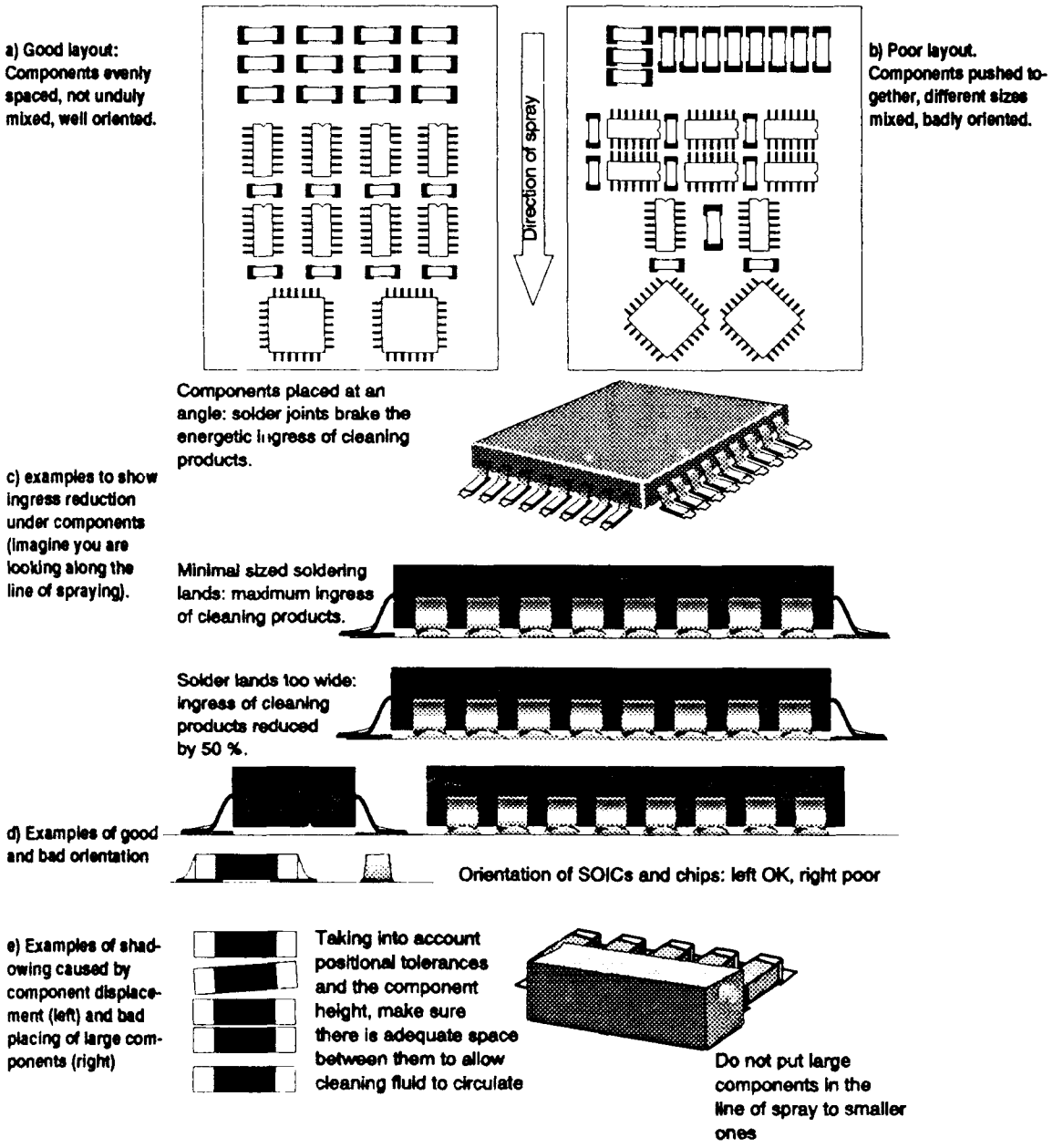

FIGURE 5. Layout Criteria for Highest Reliability

CLEANING PROBLEMS

No matter which cleaning process is used, there are certain rules common to them all. It goes without saying that the solvents should be selected for the job in hand: it is as bad to use, say, CFC-113 for removing a water-soluble flux as it is to use pure water to remove rosin. Successful cleaning is only possible if cleaning liquids, hereinafter called solvents for simplicity even if they are not solvents in the strict sense of the definition,

circulate energetically where there is contaminant to be removed. The implication is that high energy pumping, spraying, ultrasonics or any other means of circulating the solvent under the components is essential and the design of the system must take into account the topography of the circuits being cleaned. Generally, aqueous systems are as effective as purely organic methods for a given total energy level [Reference 12]. There has been a misconception in the past that the low surface tension of some organic solvents allowed a better penetration under tight stand-offs. This is only a half-truth. The penetration by capillary action is better with water than with, say, alcohol or CFC-113 but, by the same token, it is more difficult to remove the water out from under the components afterwards. Empirical tests by various persons have shown little difference in cleaning quality between different aqueous and non-aqueous processes [References 6, 12, 13].

Where possible, components must be selected with as large a stand-off as possible. The ideal minimum is approximately 0.3 mm. The main problem component is the leadless (castellated) chip carrier, often in ceramic. These are large flat components which are frequently placed horizontally on the PCB with virtually no stand-off other than the conformal asperities of the board itself. Quite apart from the difficulty in allowing the solvent to circulate under such a component, the latter exhibits two other practical difficulties: the differential thermal coefficient of expansion places undue strain on the solder joints as the laminate heats up and the solder paste frequently wets poorly in the castellations as it is not well forced up them as the component is placed on the pasted lands. All three of these problems can be resolved simultaneously by the use of an intermediate lead frame which is initially soldered to the component using a s[illegible]r paste with a melting point of about 250°C, formed and trimmed. This makes a positive low-cost contribution to the reliability of the assembly (Figure 4). Another point is that solvent trapped under such a component will evaporate very slowly, even if the assembly is elevated to temperatures higher than the solvent boiling point. Such evaporative drying is detrimental to the reliability as any dissolved residual contamination is redeposited on the circuit, frequently close to the connections. Again, using a lead frame will assist drying by allowing the residual solvent to be centrifuged or blasted out with its dissolved contamination (see below).

A frequently ignored but important aspect is the design for reliable cleaning. Component placement should be such as to always allow the maximum ingress of solvent under the components. Orientation should always be that the free space under the component is directly attacked by the cleaning system. If a spray is used, small two-land passive components (e.g. resistors and capacitors) should be across the spray, whereas SOICs should be placed with their long axis along the direction of the spray. Square chip carriers with connections along all four sides should not be oriented at 45° to the spray axis. As much as possible, keep components of a similar size in the same zones: small components lodged between tall ones will present difficulties. As far as is practicable, fill out the "real estate" as evenly as possible and avoid "clumping" of components together. The space between the components is also an important factor and should be not less than one-third of their aggregate height plus 0.5 mm, taking into account the worst-case of the mechanical placement tolerances after soldering. For this reason, from a purely cleaning point of view and without thought for the actual soldering process, pads and lands should err on the small rather than the large size. This is especially important when chip-carriers are used, as the cleaning solvents must pass between the connections (Figure 5). Along the same thought process, the autorouting design rules should be programmed not to allow leads to pass between adjacent lands of the component footprint, even if the minimal spacing is respected. Ideally, the outer layers should bear only the lands and connecting through-holes via the shortest conductor length, all the signal and power routing being on inner layers. Above all, avoid using blind holes for connecting inner layers to component pads, only through-hole vias are acceptable. Of course, buried vias are acceptable.

Another factor associated with any form of aqueous cleaning is the problem of drying [References 7, 12]. For maximum reliability, drying should be an integral part of the cleaning process. It must be assumed that, as rinsing is a number of successive dilutions, the residual water under components cannot possibly be pure, albeit not heavily contaminated. If this water is allowed to evaporate, the residues will be redeposited on the assembly close to where the capillary forces were strongest, i.e., where the connections are. This is exactly where such residues could cause the most harm. Evaporative or vacuum drying alone is therefore incompatible with high-reliability electronics. The way round this problem is to remove this slightly contaminated water mechanically, either by centrifugation or by clean air blasting: the contaminants are removed along with the bulk of the water. The final few percent of the remaining water, essentially wetting the surfaces, can then be evaporated.

Practical trials have shown that the residual contamination can be reduced by half an order of magnitude simply by using rotary high-speed air knives in a well-designed batch dryer.

Low volatility hydrocarbon derivative solvents also present drying problems and similar rules apply as with water. However, with water, it is possible to heat to any temperature up to the limits supported by the components. This is often situated at over 100°C (frequently the limit is the T_g of the substrate, typically between 100 and 120°C for quality standard FR-4 materials). With the HC derivatives, it is always recommended to keep the peak temperature at 20—25°C under the published closed-cup flash point. One such product has a CC flash point of 105°C and the manufacturer foresees drying occurring at typically 80°C, purely for safety reasons. If air knives are used, care must be taken that the solvent mist produced is not flammable or, if it is, it cannot be ignited. Such a mist or vapour is likely to be subject to a "polluters pay" tax in many countries and it is foreseen that effective removal will become necessary in most countries long before the end of the century. It would therefore be wise to specify adequate solvent elimination in the exhaust air at the time of specifying the machinery. It need not be expensive, even for small installations.

There is one fonn of post-soldering contamination that, although occasionally present on conventional circuitry, has become a real reliability problem with SMT: this is the presence of solder balls. This has two causes: poor or badly used solder paste and "no-clean" wave-soldering fluxes. The reasons that this is a particular problem with SM assemblies is that a) solder paste is almost exclusively used for these and b) the size of the balls more nearly approaches the conductor spacings usual on SM layouts, creating a more real risk of accidental short circuits. Of course, if energetic cleaning is employed, most or all the solder balls are eliminated at the same time. This is why the problem is more severe with no-clean techniques. The balls adhere loosely to the surface, to be dislodged at some indeterminate future date.

CONFORMAL COATING PROBLEMS

Once an assembly is tested and perfectly clean and dry, for high reliability applications it is usually conformally coated [References 10, 11]. There are several methods of conformal coating. The usual ones are:

- dipping
- vacuum impregnation
- brushing
- spraying
- vacuum deposition.

The last-named would seem the most reliable, where an organic monomer is evaporated under high vacuum and polymerises as it condenses on the surface to be treated. This leaves a tough, thin, even and highly resistant film on all surfaces, even under large components. The only drawback is that the process is extremely expensive. The other four processes all involve a risk of contamination being co-deposited with the coating resin. The first three entail the possibility of residual contamination from one circuit polluting the resin which is then used for subsequent circuits. Spraying, unless done with bottled gas, implies the risk of air impurities (e.g. oil and water) being co-deposited with the resin. Only all-stainless steel spray guns should be used as the more common aluminium ones are frequently attacked by certain monomers. Ideally, where an SM component is close to the substrate surface, both the component and substrate surfaces should have separate coatings. If this is not possible, then the whole space under the component should be filled with resin. The thing to avoid, at all costs, is to leave an air bubble trapped under the components. This will almost inevitably fill with water under very severe, humid, tropical climatic conditions.

Certain types of conformal coatings, particularly elastomeric silicone types, are notorious mechanical shock transmitters. If a board may be subject to high-g acceleration forces, especially along the Z-axis, the under-component space should not be filled with such coating materials. Otherwise, the component and/or solder joints may fail prematurely. Of course, this is not unique to SM components, but the small stand-offs of SM devices does tend to aggravate the problem.

Curing of conformal coatings is an essential part of the process. Correct curing can be achieved only if the mixture is stoichiometrically correct and the manufacturer's time and temperature curve is followed precisely as

a minimum curing time, but give preferably a few percent more. Ultra-violet methods of starting the curing cycle is often problematic with SM techniques.

EFFECTS OF CONTAMINATION

This subject has been dealt with in detail in the standard literature [References 10, 11]. It is a long and complex subject, outwith the scope of this paper. It is therefore simply proposed to catalogue the more dangerous results of undue contamination or inadequate cleaning.

CORROSION

Several corrosion mechanisms are known, most of which are related to the presence of ion species on the assembly.

DENDRITE FORMATION

This is probably the most frequent cause of intermittent failure after "dry" solder joints. It is the formation of microscopic and very fragile filaments between conductors of different polarity under humid or wet conditions. Ionic contamination is necessary for it to occur.

VESICATION

This is also sometimes known as "mealing". It consists of the formation of myriad minute blisters which fill with water absorbed from the atmosphere. It is caused by the presence of hygroscopic contaminant species (ionic or not) under a solder mask or a conformal coating.

SURFACE INSULATION RESISTANCE LOSS

The presence of many ionic or non-ionic contaminants may be responsible for a deleterious effect of the insulation on assemblies, potentially causing misfunctioning. Chemical attack of polymeric substances (substrate or solder mask) may exhibit a similar effect.

"WHITE RESIDUES"

There are several known causes of so-called white residues. They are all related to the presence of contaminants, improper flux selection, improper cleaning method selection or poorly polymerised laminate or solder mask (or any combination of them). There has been a recent recrudescence of such residues. This is because some users of rosin-based low-solids "no-clean" fluxes may have a few circuits where cleaning is obligatory and wish to use the same flux for both applications. This is frequently impossible. "No-clean" fluxes, as their name implies, are not designed to be easily cleaned. If cleaning of such fluxes is necessary, saponifier cleaning will probably give the best results as the flux activators are generally saponifiable where they are not soluble.

COATING ADHESION PROBLEMS

A solder mask or a conformal coating applied to a contaminated or otherwise improperly prepared surface may not adhere correctly.

COATING CURE PROBLEMS

Although, strictly speaking, not a contamination, an improperly cured laminate, solder mask or conformal coating behaves in an identical manner to contamination and may cause many of the above effects.

MATERIAL SELECTION

BASE MATERIAL

As a general rule, glass reinforced epoxy substrates to the FR-4 specification is the preferred material for the majority of quality electronics applications. Glass or Kevlar reinforced polyimide is sometimes preferred where the temperature coefficient of expansion must be better matched to that of ceramic components than is possible with epoxy laminates. From the cleaning point of view, this may be a negative factor as some cleaning methods may not be allowable (e.g. saponification, where the high alkalinity attacks the substrate). In addition, the high moisture absorption of polyimide may create electrical problems under tropical conditions with critical high-impedance circuitry.

Hybrid materials may also present some small cleaning difficulties as certain thick film glazes and thin film substrates may also be sensitive to high pH cleaning solutions.

FLUX AND CLEANING MATERIALS

The choice of the combination of flux and cleaning solvents or detergents is often made empirically or intuitively, without weighing up all the pros and cons. In truth, as far as reliability is concerned, good results can be obtained with nearly any of the usual combinations (Table 1). Nevertheless, the choice should be made only after empirical trials using a number of different fluxes and, if appropriate, cleaning products under full production conditions. Laboratory evaluation is useful only for shortlisting for full-scale production tests. Selection according to laboratory tests is foolhardy and fraught with danger. Only production tests will allow a rational decision to be made. As a general rule, rosin fluxes of the military RA types are easier to clean off, by any method, than other rosin fluxes, including some of the RMA ones. Especially difficult are the rosin fluxes that are activated with fairly massive quantities of mono- and di-carboxylic acids which are frequently responsible for the so-called "white deposits".

In terms of cleaning off flux residues, the following list gives a decreasing order of typical residual contamination *under the best production conditions with top-quality machines* and processes:

MIL-RA flux with 1,1,1-trichloroethane mixture cleaning (worst)
MIL RA flux with CFC-113 azeotrope cleaning
MIL RA flux with alcohol cleaning
SA flux with CFC-113 azeotrope cleaning
MIL RA flux with saponifier + water cleaning
Water-soluble flux with water cleaning
MIL RA flux with hydrocarbon/surfactant + water cleaning (best)

This list is obviously non-exhaustive and includes CFC-113 and 1,1,1-trichloroethane which are both controlled under the Montreal Protocol. These are given for purely reference purposes to indicate that they do not produce as good results as the substitute methods which replace them.

PRINTED CIRCUIT FINISHES

There are two finishes which bear upon the cleaning reliability. These are the type of solder mask or resist that is used and the finish on the metallic parts to be soldered.

The solder mask or resist is critical as certain types have been shown to decrease, rather than increase, the reliability. Correctly cured epoxy-based types are generally preferable and these may be either silk-screened and thermally cured or liquid photoimageable types. Some of the dry-film resists, especially aqueous types, are known to give problems because of absorption of ionic material during the development phase. This may leach out again at a later date under certain conditions, causing a loss of surface insulation resistance and a risk of ionic effects, including corrosion.

The metal finish is only a secondary consideration as, in itself, it makes little difference to the reliability, assuming that soldering can be successfully achieved with a minimum amount of rework. What is more important is the residual contamination that the metal-coating process may leave on the circuit. This is of equal

importance whether the coating is done before or after the application of the solder mask or resist. The usual contaminants which are often difficult to eliminates are metal-plating salts and/or fusing or levelling fluxes. All of these may leave dangerous levels of residual contamination if the process is uncontrolled.

CONFORMAL COATING MATERIALS

The choice of materials for conformal coatings is dependent on many factors, not the least of which is the method of application. Contrary to popular thought, all polymeric materials are more or less porous at a molecular level. The function of a conformal coating is therefore to protect the circuitry against gross contamination. It offers little long-term protection against humidity. This means that if an assembly is not perfectly clean before the coating is applied, the contamination may absorb humidity from the air, through the coating. This is almost a certain cause for a long-term loss of reliability and any failure due to this is almost irreparable.

Not all coating materials allow the passage of humidity at the same rate. Again contrary to popular thought, silicone elastomers are amongst the most prone to this problem: a test of a 5 mm thick disc of a silicone elastomer coating material, 100 mm diameter, held with air at 95% RH on one side and 5% on the other side, all at 40°C allowed the passage of 1 g/day of water vapour. This was 40 times worse than an epoxy or an acrylic coating and 20 times worse than a polyurethane one, under identical conditions.

Other characteristics that must be examined are, of course, the electrical properties, the temperature resistance, the chemical resistance, the "reparability", the requirement for primers, the flexibility, the adhesion to all materials in the assembly, the temperature coefficient of expansion, the shock transmission, the chemical compatibility to all materials in the assembly, the permissible tolerance of stoichiometry, the toxicity of the uncured products (warning! uncured polyurethanes contain toluene 2,4-diisocyanate also known as TDI, an extremely toxic and reactive substance), resistance to reversion etc. This list is more than sufficient to make one realise that the selection is a difficult process if the utmost reliability is required [References 10, 11].

CONCLUSION

Contamination may produce an important influence on the reliability of electronics assemblies. The best method of reducing the presence of contaminants on them is by qualification procedures involving different processes, followed by regular production controls. The fact that CFC-113 will be phased out shortly and must be replaced by other, possibly less benign, cleaning processes indicates that contamination control is becoming increasingly important.

WARNING

It has been shown that process qualification for high reliability may take several months or over one year. Swiss and German CFC-113 and 1,1,1-trichloroethane phase-out regulations do not leave much time for this to be done correctly. It is strongly recommended that companies who have not yet started substitute qualification must do so immediately. At this moment, equipment manufacturers have spare capacity and will welcome orders for non-ozone-depleting process cleaning machines for delivery in ample time before the regulations come into force. A delay of another six months may find that the equipment manufacturers can no longer meet delivery schedules before the deadline. It is therefore imperative that manufacturers of high reliability electronics take steps now.

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MEASURING IONIC CONTAMINATION USING TODAY'S CLEANLINESS TEST EQUIPMENT

by

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ABSTRACT

The most common method for evaluating the cleanliness level of a printed circuit assembly (PCA) is a method called the Resistivity of Solvent Extract or ROSE test. The original procedure, developed in the early 1970's, used a laboratory squeeze bottle filled with a 75% isopropanol and 25% deionized water solution to dissolve ionic contamination from the PCA into a beaker. The conductivity of the extract solution was then measured and assigned a value based on a sodium chloride (NaCl) standard.

In the last 18 years, several manufacturers have developed and marketed equipment to perform this type of testing. During that time, radical changes have been made to the systems, such as the addition of solvent heaters, sprays and microprocessors. A recent study at Motorola has shown discrepancies among, not only the different manufacturers, but also among different parameters such as solvent temperature and volume. With such a diverse selection of cleanliness test equipment available, how is a manufacturer to know which instrument to choose for his particular process? How accurate and reproducible are the results from these machines? How efficient are these systems at removing contamination from under surface mount devices? It became necessary to examine these variable parameters so that the ionic residues detected from one system could be compared to the residues detected on other systems.

The U.S. Navy's Electronics Manufacturing Productivity Facility (EMPF), in conjunction with the Institute of Interconnecting and Packaging of Electronic Circuits (IPC), has taken the initiative to develop a standard test protocol for evaluating ionic test procedures and equipment. This paper details some of the observations noted in both equipment and materials while developing the test procedure.

BACKGROUND

Residual contamination left on a printed circuit assembly (PCA) is generally classed into one of two categories: ionic or nonionic. Ionic residues, derived from plating salts, flux activators and human perspiration for example, have the ability to conduct electrical current. In the presence of moisture, these residues can cause short circuits and corrosion of solder joints. Nonionic residues, such as rosin, oil or grease, act as insulators and do not conduct electricity. This type of residue can inhibit current flow across edge connectors or some other communications port. Fluxes used in the manufacturing process contain both ionic and nonionic materials.

It is obvious that a "clean" PCA has a greater chance for reliability. In 1972, the Naval Avionics Center (NAC) in Indianapolis, Indiana conducted a study to find a technique for measuring how "clean" a PCA is after the manufacturing process.[1] The procedure used a squeeze bottle filled with 75% isopropanol and 25% water solution with a minimum resistivity of 25 megohms-cm to rinse ionic residue off of a circuit board. The extract solution was funneled into a beaker and the resistivity measured. This measurement was compared to the starting resistivity and the change equated to a NaCl standard and calculated in micrograms per square inch ($\mu g/in^2$) of board surface area. Once the quantity could be measured, NAC also established a pass/fail criteria that a circuit board must meet in order to perform its intended function in the field. The study determined that PCA's with surface contamination greater than 10.06 $\mu g/in^2$ tended to fail Surface Insulation Resistivity (SIR) testing.

Once the test method and the pass/fail criteria were established, equipment manufacturers began designing and building systems to do this type of testing. As the years progressed, advances such as solvent heaters, microprocessors, and sprays were incorporated into the systems. As the efficiency of the systems increased, it was no longer possible to compare these results to those of the old beaker/funnel technique. A PCA with ionic residue on the surface may pass a beaker/funnel test, but fail the test using a new system with heated solvent. To make the test more fair, and not penalize an ionic cleanliness tester for being too efficient, the Navy assigned "equivalency factors" to the equipment and put them into various military standards, such as MIL-P-28809 and MIL-STD-2000. The theory behind the "equivalency factors" was that the same PCA that measured 10.06 $\mu g/in^2$ using the beaker/funnel test would measure 14.00 $\mu g/in^2$ in an Omegameter, and 20.00 $\mu g/in^2$ in an Ionograph. The problem is that the Omegameter and the Ionograph are still evolving and the factors stated in the standards do not

pertain to the newer models. In addition, equipment introduced to the market after the study are not mentioned in the standards.

The problem was further complicated when Motorola noticed that the temperature of the solvent significantly influenced the final result of a test.[2] Bill Kenyon of DuPont showed that solution temperatures could increase by as much as 14° F over the course of a work day, increasing the results by as much as 20%.[3] One ionic cleanliness tester could give two different answers for the same PCA depending on the temperature of the solvent. Other studies with similar results led the IPC to form an Ionic Conductivity Task Group (ICTG) to investigate temperature and other variables involved with ionic test equipment.

TESTING

Objective

One of the primary goals of the study is to establish how the different system variables affect the removal of ionic residues from under known standoff heights. Our goal is to be able to determine that "System A", for example, with no heat and no sprays was 88% efficient at removing residue from under a 0.009 inch standoff, only 60% efficient at 0.006 inch standoff, and 30% efficient at 0.003 inch. This data could then be compared to "System B" with heat and sprays that was 100% efficient at 0.009 inch, 98% at 0.006 inch, and 85% efficient at 0.003 inch standoffs.

This study will examine the different variables that are associated with some of the newer ionic cleanliness test equipment, such as solution temperature, volume and alcohol content. In addition, various concentrations of different flux types will be used to measure how accurate each system is at detecting specific residues. Finally, stainless steel plates machined to yield known standoff heights will be used to determine the efficiency at removing residue from tight spaces.

Another target for this project will be to look at the validity of the equivalency factors assigned to some of the testers in various military standards. It is understandable that there is a need to compensate the newer, more efficient systems to somehow relate their results to the original beaker/funnel method, but how accurate are these factors? Have the factors changed over the years? What variables influence these factors?

Equipment

Equipment vendors agreed to loan their ionic cleanliness (IC) test equipment to the EMPF for the duration of the study. All of the equipment used in this study is commercially available from Alpha Metals, Kester Solder, London Chemical, Protonique, and Westek. The equipment is classed into one of four categories; Static/ No Heat, Static/ With Heat, Dynamic/ No Heat, Dynamic/ With Heat (see Table 1). The term "static" is really a misnomer in that static generally refers to something as being stagnant, or motionless. The static systems continually circulate solvent from the test tank, past a conductivity meter, then back into the test tank. Ionic residues are dissolved and distributed throughout a set volume, so the conductivity of the solvent will climb and then level off (see Figure 1).

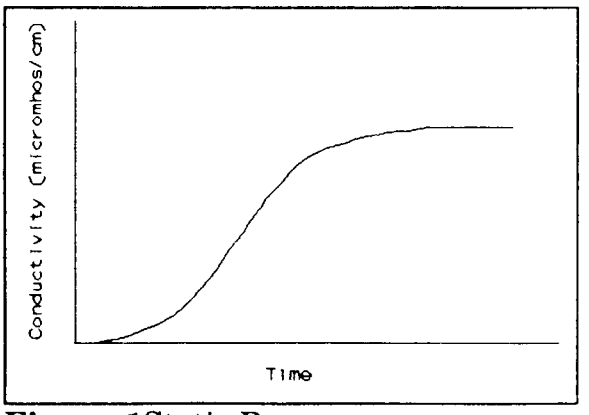

Figure 1 Static Process

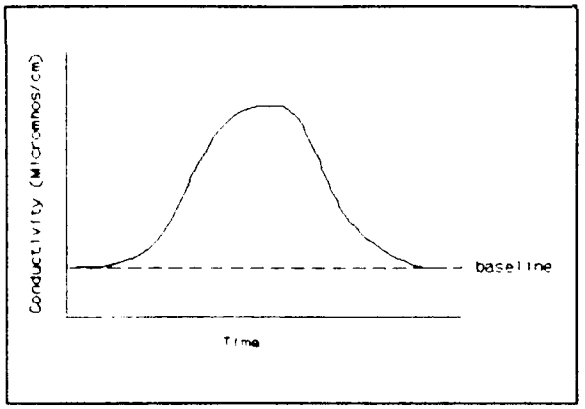

Figure 2 Dynamic Process

The "dynamic" process takes solvent from the test tank, measures the conductivity, deionizes the solvent, and then puts it back into the test reservoir. Because contaminated solvent is being replaced with clean solvent in this type of testing, the conductivity reading starts at a baseline, climbs as the residue is removed, then returns to that baseline as the solvent is deionized (see Figure 2). The area under the curve is then used to measure the total ionic contamination.

Operation of the equipment will be based upon standard operating conditions set by the manufacturers and some preliminary work done at the EMPF. Any changes to the operating procedures are recommended by the manufacturer to the EMPF, with final approval coming from the ICTG.

TABLE 1 EQUIPMENT CLASSIFICATIONS					
COMPANY	MODEL	TYPE	HEAT CONTROL	VOLUME CONTROL	SPRAY
Alpha Metals	Ionograph 500SMD	Dynamic	Yes	No	Yes
	Ionograph 500M	Dynamic	No	No	No
Protonique	Contaminometer	Dynamic	No	No	No
Lonco	Zero Ion	Dynamic	No	No	Yes
Westek	Icom 5000	Static	Yes	Yes	Yes
Alpha Metals	Omegameter 600SMD	Static	Yes	Yes	Yes
	Omegameter 600R	Static	No	Yes	No
Kester Solder	Ionex 2000 100	Static	No	Yes	Yes
	Ionex 2000 300	Static	No	Yes	Yes
Protonique	Contaminometer	Static	No	No	No

Test Vehicle

The test vehicle used to determine the ability of a system to remove ionic contamination from under known standoff heights is pictured in Figures 3 and 4. The board (Figure 3) consists of an FR4, epoxy/glass laminate with .5/.5 ounce copper patterns. Stainless steel plates (Figure 4) were machined to yield a known standoff height of 0.003, 0.006, or 0.009 (+/- 0.0005) inch. Four stainless steel coupons, all with the same standoff, are mounted to the board using stainless steel nuts and bolts. For consistency

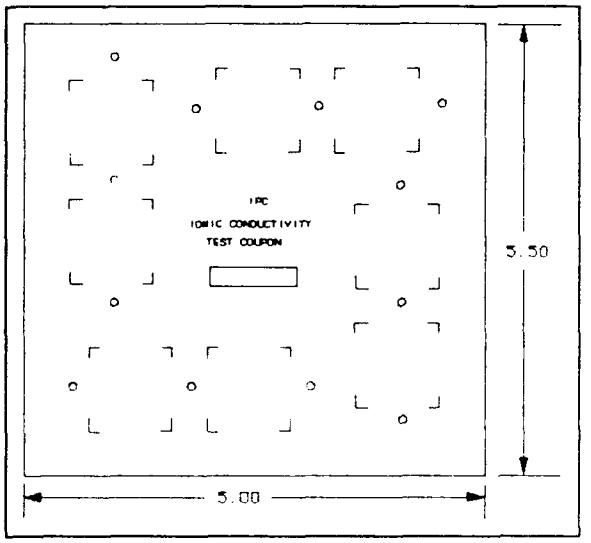

Figure 3 ICTG Test Board

throughout the study, all of the nuts used to hold the plates to the test boards will be torqued to 5 inch/pounds.

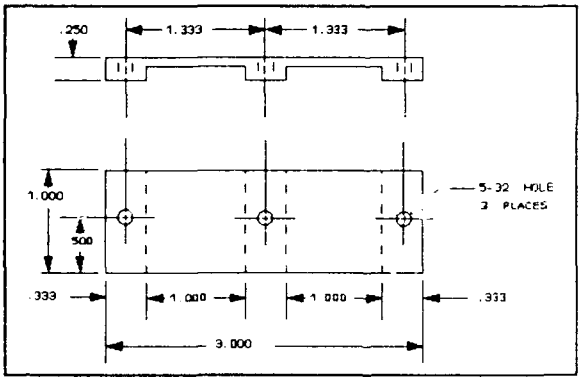

Figure 4 ICTG Cover Plate

Flux Types

The consensus of the ICTG was to not use commercially available fluxes in this study due to the fact that all fluxes dissociate and ionize differently based on their chemistries. Instead, two formulations of "fluxes" were used as a standard in which to compare the test equipment. The two formulations were made of the following ingredients:

Strongly Ionizable "Flux":	60% Isopropyl Alcohol 5% Diethylamine Hydrochloride 5% Malic Acid 5% Triton X100 15% PEG 600 10% Deionized Water
Weakly Ionizable "Flux":	75% Isopropyl Alcohol, 20% Water White Rosin, 5% Adipic Acid

A microliter syringe is used to dispense the "flux" within the boundaries of the eight, 1"x1" squares printed on the board. The volume was kept constant at 5 microliters per 1 inch square (40 microliters total) throughout the testing. The concentration however, was diluted with isopropanol to give three different contamination levels. The three levels originally defined were 5, 15 and 25 $\mu g/in^2$ of NaCl equivalent, which equates to 40, 120 and 200 total micrograms respectively, based on an eight square inch area. These levels were later increased to 5, 30 and 55 $\mu g/in^2$ in order to cover a broader range of contamination.

OBSERVATIONS

One of the primary goals of the study is to establish how the different system variables affect the removal of ionic residues from under known standoff heights. In order to do this type of testing and draw legitimate conclusions, it is essential that all test assemblies have the exact same amount of residue. It is also important to know what that quantity is in order to determine the accuracy of the ionic test equipment. Though this sounded relatively simple at first, it proved to present a problem. A known volume of residue could be deposited onto the substrate using a microliter syringe, but what volume of "flux" does it take to make a set amount of NaCl equivalent? Additionally, that volume of "flux" had to be physically placed within eight, 1"x1" square areas. It was established that 5 microliters could be dispensed within a 1"x1" square area, and since the test board had eight squares, a total of 40 microliters could be dispensed onto the test vehicle. So a flux volume of 40 microliters had to equal the resistivity change of 5, 30, and 55 $\mu g/in^2$.

One ionic cleanliness system was randomly selected to be the test instrument. A NaCl standard was made so that 40 microliters would equal 80 micrograms of NaCl (10 $\mu g/in^2$ based on an 8-square-inch area). The idea was to take the system to a known resistivity and inject 40 microliters of solution directly into the test tank. The change in resistivity would represent 80 micrograms of NaCl equivalent. The system would then be returned to the same starting resistivity and the "flux" titrated into the test cell to that same ending resistivity. The volume of "flux" titrated would be 80 micrograms of NaCl equivalent.

The first problem revealed test results that were lower than expected and not repeatable. Further research found that the system has what was termed a "dead band" area. The resistivity probe has a limited range and, though the solvent could be cleaned to a higher resistivity, the system would continue to read the maximum limit of that probe. For example, the starting resistivity was thought to be 50 megohms-cm, but the actual starting point may actually have been 70, 95, or 120 megohms-cm. Contamination removed from the PCA was not measured until the resistivity of the solvent was within the range of the probe. To achieve accurate readings, it is necessary to have a starting resistivity within the range of the probe so that all contamination removed from the PCA can be measured. This problem was not unique to one system, but instead was typical for most of the equipment tested. Some exhibit the problem to a lesser degree than others, and some have software which stops circulating the solvent once the resistivity gets to the limit of its probe. In addition, this problem is more noticeable in the static systems than the

dynamic. The "dead band" area may influence the readings of any one of these equipments if the operator was not careful or was not aware of the problem.

Once the "dead band" problem was solved, the next observation was that the readings were now higher than the expected 10 $\mu g/in^2$ and the results seemed to be volume dependent. Three different volumes were used in the test cell and the results averaged 12.5, 14.8, and 16.2 $\mu g/in^2$ NaCl equivalent. A second cleanliness tester was used to verify the results of the first system and it was noted that the volume did not influence the results; however, the results were nearly twice what was expected (about 20 $\mu g/in^2$). At first it was theorized that the isopropanol used to make the standard was contributing to the change in resistivity therefore contributing to the contamination. A blank was run on the first system and the result was 2.0 $\mu g/in^2$. The blank for the second system was 20 $\mu g/in^2$ and a further test in which nothing was added to the test cell resulted in 20 $\mu g/in^2$. A look at the printout of the second system showed that the results were 0.0 $\mu g/in^2$ for the first minute of testing, but then jumped to 8-12 $\mu g/in^2$. In addition, the printout showed that the results slowly and steadily increased from that point throughout the duration of the test and stopped at 20 $\mu g/in^2$. Three more questions had arisen:

1. Why did the results jump at one minute?
2. Why did the results gradually climb?
3. Why did the climb stop at 20 $\mu g/in^2$?

The gradual climb in the readings was thought to be caused by carbon dioxide (CO_2) absorption. To test this theory, nitrogen was fed into the test cell to form an inert atmosphere over the solvent/air interface. Results showed that the gradual climb had been eliminated, but there was still a jump at one minute. The jump was causing the results to be 3.0-7.4 $\mu g/in^2$ even though no contamination was being introduced into the test cell. The jump was not consistent and, after closer examination of the printout, it was noted that the jump was dependent on the starting resistivity of the solvent. Unlike the first system that subtracts the ending resistivity from the starting resistivity and calculates contamination based on that change, this system assumes a starting point (which is the maximum upper limit of the probe) and at one minute, subtracts the resistivity from the assumed starting point and calculates the contamination based on that change. To verify this theory, the solvent's resistivity was adjusted to match the assumed starting resistivity under a nitrogen blanket. No contamination was added and the test resulted in a reading of 0.0 $\mu g/in^2$.

The third question was answered when it was learned that the

termination of the test is dependent upon the range at which the printer is set. If the results of the test go higher than the printer range, the test will terminate. It was no coincidence that for all five conditions tested (three NaCl standard, one blank, and a zero) an identical reading of 20 $\mu g/in^2$ resulted. The CO_2 drove the reading up off of the printer range, which was preset for 0-20μg scale, and terminated at 20 $\mu g/in^2$.

It appears that the only way to get an accurate number with this particular system is to create an inert atmosphere inside of the test cell, start at a point no higher than, but no lower than the maximum range of the resistivity probe, and not exceed the maximum range of the printer. But if testing thus far is accurate, why have these problems not been noticed before? As mentioned earlier, the surface area of the test vehicle was set at 8.0 square inches. This small surface area magnifies the imperfections of the test equipment. A change in resistivity represents a certain amount of total contamination. If the change in resistivity correlates to 100 micrograms, for example, and the surface area is 100.0 square inches, the result is only 1 $\mu g/in^2$. If that same resistivity change was measured for a surface area of only 1 square inch, the result would be 100 $\mu g/in^2$. A deviation in resistivity readings of 50% would insignificantly change the larger surface area by 0.5 $\mu g/in^2$. The resulting change of 50.0 $\mu g/in^2$ for the smaller area would be much more noticeable.

Once a blank could be established with a reading of 0.0, testing resumed. Again, the NaCl standards were made and the change in resistivity was measured. The "flux" was then titrated to that same resistivity change to establish how much "flux" it took to make that NaCl equivalent. As noted earlier, the volume of contamination was to be kept consistent and by diluting the original stock solution properly, all three contamination levels could be produced in 40 microliter increments.

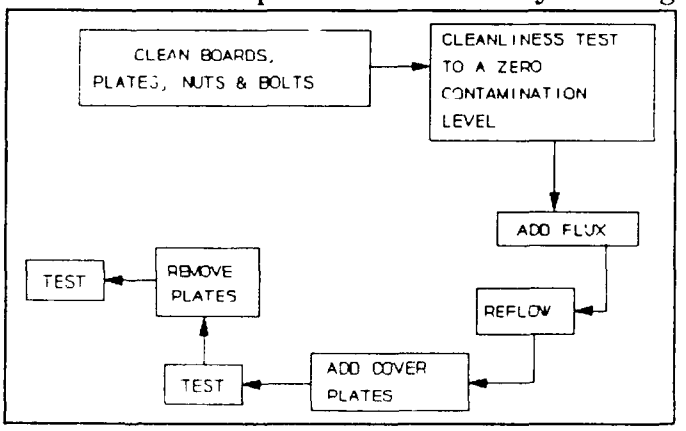

Figure 5 Test Coupon Preparation

The next task was to develop a process flow for the coupons. Again, this seemed to be fairly simple at first: clean the assembly, put a known quantity of flux down, bake the flux onto the assembly, then determine if the ionic cleanliness tester

gives accurate and reproducible results (see Figure 5). The original process selected to bake the flux onto the test vehicle was infrared (IR) reflow with a thermal profile similar to that of the IPC Chlorofluorocarbon Alternative study.

Early test results with this process flow proved to be inconsistent and lower than expected. A total of 40 microliters of the first "flux" standard was deposited on each of ten different bare boards. The boards were reflowed on the same machine at the same identical thermal profile, and yet the results varied considerably. The investigation of this problem used 40 microliters of straight "flux", thereby removing the possibility that the error was due to mixing or handling of the standards. Further modifications to the thermal profile, including the addition of one and two prebake steps found that the results were very dependent on temperature (see Table 2). Depending on how the flux is heated, results varied from 0 to 2800 total micrograms using the same ionic tester.

TABLE 2 IONIC CONTAMINATION VS TEMPERATURE

PROCESS	AVERAGE TOTAL μGRAMS	RANGE	MEASURE OF PRECISION
Wet Flux, Directly into Test Cell	2802.1	35.6	.0127
Wet Flux on Board, No Heat	2805.2	236.3	.0842
Flux on Board, 1 Hour at 45°C	2436.8	150.4	.0617
Flux on Board,1 Hour at 45°C, 1 Hour at 100°C	1607.0	426.5	.2654
Flux on Board, IR Reflow Only	471.1	309.0	.6559
Flux on Board,, 1 Hour at 45°C, IR Reflow	356.8	414.0	1.1603
Flux on Board, 1 Hour at 45°C, 1 Hour at 100°C, IR Reflow	279.8	107.8	.3853

**** Measure of Precision (MOP) = Range divided by Average**

After consulting with industry flux experts, the consensus was that flux will volatilize, oxidize and polymerize depending on a number of different variables. Though 40 microliters was dispensed on each board (5 microliters per square), each deposit has its own geometric shape (see Figure 6). A 5 microliter spot that spreads thin, as shown in example #1, will completely volatilize and, if given enough time and/or temperature, will polymerize and become insoluble in alcohol/water. On the other hand, a spot that does not spread, as shown in example #2, may polymerize a "shell" over the surface of the flux, and trap wet flux inside. Once this "shell" is dissolved, the rest of the flux would break down and ionize quickly.

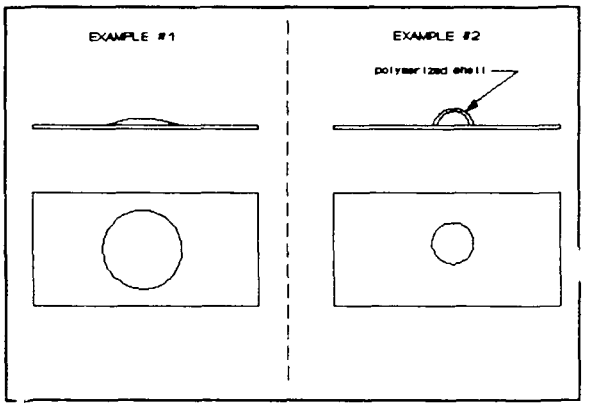

Figure 6 Flux Geometry

In addition to the physical geometry of the sample, the chemistry of flux changes when exposed to elevated temperatures due to volatilization of the weak acids. These weak acids would normally contribute to ionic contamination readings when the flux is wet, but as these acids evaporate, the resulting NaCl equivalent is lowered. The degree to which this volatilization influences the final result is dependent on how thick the "shell" is and how quickly that "shell" formed.

All of the testing mentioned thus far has been done on the strongly ionizable "flux" only. This is due to the fact that the strong "flux" was supposed to break down and ionize easier than the weak "flux". What little weakly ionizable "flux" testing that has been done up to the time this paper was authored has shown that it is indeed less predictable.

CONCLUSIONS

Research so far has shown that evaluating cleanliness test equipment is a little more complicated than putting a known quantity of residue under a known standoff, measuring the residue, and determining how accurate the system is. Known quantities of wet flux could be used, but to relate efficiency of the system to a real world situation, the flux must be heated. On the other hand, it is also important to know how much residue is on the vehicle before testing in order to know how accurate the systems are.

Conclusions that can be drawn from the preliminary testing are:

1) The ROSE test is very operator dependent.

2) Flux exposed to elevated temperatures and/or time will significantly influence the ionic reading of any system. Evaporation and polymerization occur each time the flux is exposed to heat, and those changes increase as temperature increases.

3) Solvent temperature does influence the amount of ionic materials that will dissolve and ionize into solution.

4) All of the ionic cleanliness testers, even the unheated systems, will generate some change in solvent temperature due to friction while being circulated. Most will increase only about 10-15°F, but one system, without heating elements, went from 72°F to 128°F in just over one hour. This system has since been modified and will still heat to about 105°F, but will level off at that temperature using a heat exchanger and a fan. Unlike the heated systems that can stop circulating, but still hold temperature, this system will hold temperature only as long as the pumps are circulating solvent.

5) The heated systems will stabilize at about 110°F, but the operator must wait until the solution temperature is stable.

6) Each system has its own way to calculate contamination based on the resulting data. For example, two systems could both measure the same resistivity change, yet give different answers.

7) Carbon dioxide will be absorbed by the solvent and will influence ending ionic conductivity results. Some systems try to compensate for this absorption, but they use a flat compensation that does not take into consideration solvent volume or temperature.

8) Most of the systems have a "dead band" range that can influence the final ionic conductivity results. This "dead band" is very significant in some systems and has very little significance in others.

9) Small PCA surface areas will magnify errors in process, operator or equipment.

10) It will be hard to draw meaningful conclusions or detect any trends on the weakly ionizable flux. This "flux" is very hard to ionize and is very sensitive to process variables.

11) Though solvent volume is figured into the calculation, volume does seem to influence the results of at least some of the static systems.

It is important to remember that this equipment was not developed to be an analytical tool, but instead, developed for process control. Though observations made so far appear negative, it merely shows that there is much to be known about these systems. Even with CO_2 absorption, temperature influences, and the "dead band" area, if run consistently, these systems are valuable process control tools. Operator instruction and consistency are important to detect any trends or change in materials handling, cleaning system operation, and perhaps even thermal profiling of fluxes. There are more accurate ways to measure ionic residues, but these systems are expensive and require trained laboratory analysts. The accuracy of the ionic cleanliness test equipment is continually being improved and will most likely always have a place on the manufacturing floor.

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Tim holds an AA degree from Cerro Coso Community College, Ridgecrest. He is involved in the Navy's Best Manufacturing Practices Program and is an active member of several IPC committees. He is Vice-Chairman of the Acoustic Energy Cleaning Committee.

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AUTOMATED INSPECTION AND PROCESS CONTROL FOR MILITARY SURFACE MOUNT ELECTRONIC ASSEMBLY

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ABSTRACT

McDonnell Douglas Electronic Systems Company, Lasers and Electronic Systems Division (MDESC-L&ES) recently began production in a new production facility for surface mount electronics. This production facility is the result of eight years of development of a coefficient of thermal expansion (CTE) compatible printed wiring board (PWB) and heat sink system, and two years of equipment selection and process development.

The facility provides capabilities for board preparation, laser marking, automated board feed and setup, solder paste application, adhesive application, component placement, convection/infrared reflow soldering, zero ozone depletion defluxing, repair, module assembly, inventory control, component traceability, and automated inspection/process control.

The automated inspection system is a three dimensional vision system which constructs a model of each solder joint. The three dimensional model is processed through analysis algorithms to judge joint acceptability. MDESC-L&ES is corroborating machine accuracy and repeatability with human results in a team effort involving DPRO and company Category C and Category H personnel. More importantly, MDESC-L&ES is monitoring parametric measurements from the solder joint inspection system on a mainframe statistical process control system. Process trends are reported to upstream processes in near real time via electronic monitors located at each process work area. This effort is directed towards reducing, and later eliminating, 100% solder joint inspection.

INTRODUCTION

The primary reasons many military programs utilize surface mount technology instead of plated through hole designs are increased reliability, increased packaging density and decreased system cost . Eight years of independent research and development yielded a printed wiring board and heatsink system that is CTE compatible and thereby increases the long term reliability of the electronic assembly. With proper selection of assembly equipment, and proper process characterization, the surface mount assembly process becomes almost fully automated producing very few defects. The resulting reduction in solder joint rework not only reduces the cost of assembly but also increases the reliability of the product by eliminating potentially damaging thermal cycles and thermal shocks to the assembly. An accurate and repeatable automated inspection system facilitates process control by acquiring consistent, accurate measurements on process performance that are vital to tight process control.

PARAMETRIC MEASUREMENT

Utilizing a laser to perform surface mapping of each individual solder joint, the automated inspection system builds a three dimensional model of each joint. The surface measurments are accurate to within 0.000125 inches, allowing very precise calculations of wetting angles at all edges of the solder joint, length width and height of the solder fillets, solder volume within the joint and other critical parameters. For each different solder joint family, between 60 and 180 individual parameters are measured for each solder connection. From those parameters, the most critical for each joint type are extracted and charted. The routines designed to extract this data produce process control charts in near real time on electronic monitors located at each piece of process equipment. As the operators at each piece of assembly equipment receive the feedback , adjustments are made, where necessary, to prevent the process from producing defective hardware.

A TEAM EFFORT

In order to reach the goal of replacing 100% visual inspection with automated inspection and data collection, significant cooperation had to be obtained from Quality Assurance. For military contract work, this includes both internal Quality Assurance management and resident DPRO representatives. Their participation in the project started when the equipment was first received so that each of these organizations would have a maximum satisfaction level in the performance of the automated inspection equipment and the data trend analysis. A team of representatives from all responsible areas oversaw the development of the criteria to be used for system acceptance and transition into full time production hardware evaluation. Team members included MIL-STD-2000 Category C and Category H personnel from Manufacturing Engineering, Quality Engineering, Production Engineering, Training and Quality Assurance Management and DPRO representatives.

SOLDER JOINT ACCEPTANCE CRITERIA

The initial charter of the team was to agree upon a set of dimensional criteria that the vision system would use in its algorithms to differentiate between acceptable and unacceptable solder joints. The guidelines used for these dimensional criteria came from WS-6536E, MIL-STD-2000, MIL-STD-2000A and internal studies on reliability for surface mount solder joints conducted over a four year period. In some specific cases, the work done to produce a CTE compatible printed wiring board and heat sink system provided significant data on the desired solder volumes and fillet shapes required for long term reliability.

ACCURACY AND REPEATABILITY ASSESSMENT

The next task for the team was to determine the accuracy level and repeatability level at which the system would be deemed capable of inspecting production hardware with a high confidence level in the results. Previous studies have shown the repeatability level of a given human inspector to be in the 60-65% range. Principle reasons for error are fatigue and the limits of human judgement abilities. The team felt that an automated measuring system should have both the resolution and consistency to achieve 98% or higher in both accuracy of calls and repeatability. Once the vision system has proven its ability to analyze solder joint criteria, the more important application of the system is its capability to monitor individual measurements the system uses to perform the analysis and then control the manufacturing processes based on those individual measurements.

Any manufacturing process will produce some distribution of product variance. Monitoring the shifts from the desired mean of that distribution allows a process correction to be made as a trend develops. If those corrections are timely and effective, defects in the resultant products will be avoided. In the world of military electronics assembly, this is a concept that has been discussed for years but seldom implemented with any great success. In most instances where Statistical Process Control has been used, either the internal Quality Control function or the customer or both have staunchly insisted upon 100% human visual inspection of all hardware, regardless of the defect rate history for the product. Confidence in the performance of the vision system was the critical hurdle to cross in order to allow automated inspection to actually replace visual inspection and not simply serve as a verification of the inspectors competence.

VISUAL VS. SYSTEM INSPECTION

Determining the accuracy of the calls made by any automated inspection system invariably requires that the systems calls be compared to a set of calls resulting from visual inspection by one or more humans. The team's effort to measure accuracy involved inspection of a sample board by seven individuals certified to MIL-STD-2000 as either Category C or Category H, by two inspectors certified as Category D, by two DPRO representatives certified as Category H and by the vision system. Each participant was asked to rank every solder joint into one of five groupings - insufficient solder, minimum allowable solder volume, acceptable solder volume, maximum allowable solder volume, excess solder. In addition, the presence of any other defect, such as poor wetting, peaks or pits, was noted along with the location of the defect. A composite of the human inspections was used as the baseline for comparing to the vision system. It should be noted that although there was initially a consensus among the group on only 34% of the 300+ solder joints in the sample, further discussion and examination brought the group to consensus on all but two solder connections. Since the disagreement on those two solder connections was between acceptable solder volume and minimum solder volume, the joints were considered to be 'good' and calls made by the vision system were considered as incorrect calls only if it called the joint insufficient.

CORROBORATION OF SYSTEM TO HUMAN INSPECTION

Corroboration of the system accuracy to the human calls required several inspections of the sample by the system so the parametric measurements in several critical areas could be analyzed. For example, all of the solder volume measurements made by the vision system on solder joints that the team had called excessive were grouped together to establish the range of volumes that the system should call excessive. That process was repeated for each of the other four categories of solder volumes ranked during the human inspection process. These ranges are then established within the system software through settings called 'ranking values'. Ranking values are then used by the system software in algorithms to make decisions on whether a solder joint is acceptable or unacceptable.

THE NEXT STEP

After the team is satisfied with the accuracy and repeatability of automated inspection, visual inspection of solder joints will cease. As both the vision system and the production equipment generate track records displaying process control and very low defect rates, sample inspections of each lot by the vision system will replace 100% automated inspection. Following that, the team has set a goal of abandoning the inspection concept, that of finding defects after the fact, in favor of pure process control. Using the parametric data from vision system analysis, the process will be maintained within historically proven ultra low defect limits. Any form of "buyoff" through an inspection method would become nothing more than an inefficient and expensive waste of labor.

PROCESS OPTIMIZATION

The accuracy and resolution capabilities of the vision system, along with the parametric data captured, made it an excellent tool for process control. Equally important was the use of those same features to collect the data needed for process optimization through the use of designed experiments. By measuring the volume of solder paste after stencilling and prior to component placement, the performance of the solder stencilling operation is evaluated. After placing components and reflowing the assembly, the resulting solder joint quality was compared to the relative volume deposited in order to drive the entire process toward optimum solder joints.

PROCESS CONTROL

Evaluating stencilled solder paste prior to component placement on a sample of each lot processed creates the first records for the SPC system. Comparison of solder deposit measurements to historical data for the same board style tells the operator if results similar to past successes will be expected on the current lot. Volumetric comparison of the solder deposited on randomly selected joints on any given board to the expected solder amount derived in designed experiments tells the operator and the responsible engineer the current performance level of the stencilling equipment. Solder print height that exceeds the calculated control limits generates immediate causal analysis and appropriate corrective action. Similar corrective action results from an identified trend that has not yet crossed the control limits.

The data collected during automated inspection after reflowing the solder verifies proper solder volume from the stencilling operation and provides feedback on the success of the reflow process. Obtuse angles measured at the solder-lead, solder-pad or solder-castellation interface combined with less than maximum solder volume indicate either a correction to the reflow profile is needed or a solderability problem exists with the components and/or PWB.

LONG TERM PERFORMANCE

While the development of a new process shows great promise, the proof of its worth is in daily operation in the manufacturing environment. The equipment must perform the technical tasks consistently without needing full time engineering support. The production quantities run to date have proven the capability of the system to meet the technical requirements of accuracy and repeatability. Much larger quantities are scheduled for the next year. This test of system will also provide a continuous flow of data for process improvements. Publication of the results of this year long production run is planned for late 1992.

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THE ENVIRONMENTAL IMPACTS OF ALTERNATIVES TO OZONE DEPLETING SOLVENTS

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ABSTRACT

The environmental impacts of alternatives to ozone depleting solvent cleaners were examined in this investigation. The focus of the program was to identify alternative cleaners without ozone depleting potential that would meet Raytheon's needs for the cleaning of Circuit Card Assemblies (CCA's). Technologies evaluated were saponified aqueous cleaning systems and semi-aqueous cleaning systems. Rinsewater samples from the two referenced technologies were sampled and analyzed for a variety of parameters including BOD, COD, pH, oil & grease, flashpoint, and heavy metals. Analytical testing of the rinsewaters determined that in both technologies the rinsewaters require treatment prior to disposal.

INTRODUCTION

In response to increasing evidence of the depletion of the ozone layer by solvent cleaning chemicals and the large volumes of these solvents that Raytheon uses, a task force was created to evaluate effective alternatives to ozone depleting solvent cleaners. The initiative is called The Alternate Cleaning Technology Committee or ACT and was formed in May 1990 by the Raytheon Executive Office of Manufacturing and Environmental Quality. The committee consists of representatives from 15 Raytheon facilities, thus forming a company-wide, multi-divisional initiative with thirty-five members.

The objective of the ACT Initiative is to eliminate ozone depleting solvents, Freon 113, and 1,1,1 Trichloroethane for the cleaning of Circuit Card Assemblies (CCA's) by the end of calendar year 1992.

Six main requirements were established by the ACT Committee and were used to determine what alternate cleaners would be viable for consideration in the Act Initiative. The six requirements are listed below:

- Must not degrade reliability
- Non ozone depleting
- Environmentally acceptable
- An effective cleaner
- Save alternative
- Currently available

Using this list of requirements, the ACT group conducted an equipment and chemistry survey throughout the industry to determine what types of alternative cleaners would be evaluated. The next generation of solvent cleaners, or HCFC's, were ruled out because of their uncertain regulatory future and ozone depleting potential.

The alternate cleaner could not degrade the reliability of our sophisticated military electronics product line. High levels of cleanliness are required to ensure long term reliability.

The alternate cleaner had to be environmentally acceptable which meant we did not want to solve one environmental problem and create another. Using that reasoning, rinsewaters were sampled during all tests of alternate cleaners to determine the environmental impact those rinsewaters would have on our waste treatment facilities and the environment.

The alternate cleaners had to be an effective cleaner. Here at Raytheon we work under a variety of military specifications and high levels of cleanliness are mandatory in order to ensure consistent high quality and reliability.

The alternate cleaners had to be safe for our workers. Corporate Health and Safety was a member of the ACT Committee to evaluate the cleaning chemistries that were identified. These involved the evaluation of potential health impacts of compounds such as glycol ethers and some of the new citrus based compounds in the terpene family. Also considered were the potential flammability issues of the alternatives such as the terpene based cleaners that are combustible liquids. Fire detection and suppression systems were fully evaluated.

The alternate cleaner obviously had to be currently available on the marketplace in sufficient quantities to meet Raytheon's near-term manufacturing and cleaning needs.

Once the cleaning equipment and cleaning chemistries had been selected by the ACT Committee for consideration, the next phase involved the development of a detailed cleaning process specification which would be used for the evaluation of all the cleaners and chemistries. Included in this evaluation was an environmental test plan and health and safety evaluation of the combinations of cleaner and chemistries.

The goal of the ACT Initiative was to identify an effective alternate cleaning procedure that will meet the near and long-term needs of Raytheon in the cleaning of CCA's to military specifications. A solution was needed both for in-line and batch type applications. Based on the findings in the ACT

Initiative for CCA cleaning, it is expected that these findings will help to accelerate the phase-out of ozone depleting solvent cleaners in other cleaning applications such as machining, bench top, etc..

EXPERIMENTAL PROCEDURE

The first step of the ACT Initiative was to identify the cleaning equipment manufacturers that would be evaluated in the Phase I program. A total of ten cleaning equipment vendors were identified for the Phase I evaluation. The semi-aqueous cleaning chemistries that were included in the evaluation were the terpene compound EC-7R which is made by Petroferm, Inc., and Axarel-38 which is manufactured by Dupont. The saponified aqueous cleaners were made by Kester, Federated Fry, and Alpha Metals.

The second task of the ACT Initiative was to design and fabricate a test board that would represent the Raytheon product line and provide a viable testing vehicle for the alternate cleaners. The final board design was a mix of plated through hole (PTH) and surface mount technology (SMT), measuring four inches by seven inches in size and consisting of two different substrates, Epoxy G-10 and Polyimide.

The next task was to develop a cleaning process specification which would provide a formidable cleaning challenge for the alternate cleaners. The challenge would be significantly greater than any that would be encountered during a production process, which would allow the alternate cleaners to be ranked based on levels of cleanliness. The EPA/IPC/DOD Phase II testing protocol was integrated into the specification for reasons of comparison and customer acceptance.

The cleaning baseline against which the alternate cleaner would be referenced was an existing cleaning process which used 1,1,1 trichloroethane, followed by a deionized water rinse (2 megohm) and completed with an isopropyl alcohol rinse.

The cleaning process specification involved hand soldering of the SMT devices on-site at the cleaning vendor, followed by a one minute immersion in Kester 185 RMA flux, followed by wave soldering with pre-heat topside temperature of 220 degrees Fahrenheit and a wave solder temperature of 500 degrees Fahrenheit.

The boards were then allowed to dwell one hour after which they were processed through the cleaning equipment. Thirty boards of each substrate, G-10 and Polyimide, were processed for each cleaning evaluation.

Following the cleaning process, 15 boards were visually examined for flux residue and the remaining boards were packaged and returned to Raytheon laboratories for surface insulation resistance (SIR) testing. Each board contained 5 SIR patterns for testing purposes. Upon completion of the SIR testing, a total of 840 components were cut, lifted and the board under the part was visually inspected for residual rosin contamination. Ionic residue was determined with the Omegameter and organic residues were identified using High Pressure Liquid Chromatography (HPLC).

A Phase I environmental test plan was developed to identify parameters that would be tested in the rinsewaters during the Phase I ACT testing program at the vendor sites. The environmental plan called for taking a representative composite sample of the rinsewaters during cleaning, and testing the rinsewater for the presence of five heavy metals, lead, tin, copper, nickel, and zinc.

In addition, rinsewater samples were tested for Biochemical Oxygen Demand (BOD), Chemical Oxygen Demand (COD), total suspended solids, pH, flashpoint, and oil and grease. The samples were taken at the vendor sites throughout the country and express mailed back in coolers to an analytical laboratory in Massachusetts for testing. The environmental objective of sampling the rinsewaters was two-fold; first was to evaluate the quantity and quality of the rinsewaters that would be generated from the cleaning equipment and second to evaluate those rinsewater streams for potential closed-loop processing during installation in the Raytheon facilities. The wide variety of wastewater discharge outlets at Raytheon facilities nationwide necessitated the evaluation of a number of treatment technologies for effective treatment of the rinsewaters. Another key element of environmental information that needed to be gathered during the ACT testing protocol was to perform detailed material balances of all the cleaners used in the alternate cleaning methods and determine their fate in the form of fugitive air emissions, stack air emissions, wastewater discharges, or off-site shipment as hazardous waste.

RESULTS AND DISCUSSION

Of the multiple combinations of cleaning equipment and cleaner chemistries evaluated in the Phase I ACT Initiative, three of the processes using semi-aqueous cleaning solvents were equal to or better than the 1,1,1 Trichloroethane, DI water, IPA rinse baseline. In addition, one saponified aqueous in-line system cleaned effectively in the aqueous mode. The Electronic Controls Design (ECD) 6307/6300 cleaning equipment and Accel's Microcel II are viable for batch semi-aqueous cleaning processes. These two machines were used in combination with EC-7R citrus based cleaner.

The ECD system utilizes two dishwasher style units and an auxiliary circulating oven for drying. The Accel machine incorporates a technology which spins the part to be cleaned about its center of gravity and utilizes centrifugal force to remove material from beneath components. This cleaning process is known as spin under immersion.

The Detrex Model SA-20 and Hollis Automation Hydro-Station 332 are viable for in-line processes. The Detrex unit can be utilized either in the aqueous or semi-aqueous mode, however, the machine was evaluated in the semi-aqueous configuration only using Axarel-38. To date, our evaluation has not tested the Detrex machine in the saponified aqueous mode. The Hollis Automation Hydro-Station 332 was used in conjunction with Federal Fry 3555 in the saponified aqueous cleaning mode.

The degree of cleaning was determined to be equipment dependent. This was more evident for saponified aqueous cleaning systems than semi-aqueous systems. Although, all the aqueous chemistries were similar, only the Hollis Automation unit could clean well enough to fulfill the test requirements.

The environmental findings determined that the rinsewaters from both saponified aqueous and semi-aqueous cleaning processes require treatment prior to discharge. Our results indicated that the BOD, COD, and oil and grease limits of the semi-aqueous cleaners in particular, are well above the allowable discharge limits in most parts of the country. The in-line rinsewater discharge quantities averaged 2 - 3 gallons per minute for running DI water rinse, while the batch semi aqueous cleaning processes involved the discharge of between 3 and 15 gallons per batch.

The in-line saponified aqueous system which averaged approximately 4 - 5 gallons per minute had a BOD, COD content of 9,295 milligrams per liter (mg/1) and 8,830 milligrams per liter (mg/1) respectively, with an oil and grease content of 419 milligrams per liter (mg/1). Generally, acceptable discharge values for BOD average 250 mg/1, with COD seldom listed as a discharge parameter. Oil and grease acceptable values range between 100 and 150 mg/1. In addition, the pH of the rinsewater from the aqueous treatment system was 10.9 which is slightly above allowable limits of 5.5 - 9.5 pH.

There is a significant difference between the handling of the waste wash sumps for aqueous and semi-aqueous systems. The semi-aqueous cleaning baths are reported to be very resilient and able to assimilate large quantities of rosin based fluxes prior to requiring disposal. A steady state equilibrium is apparently achievable, where drag-out of flux residues equals the volume of flux drag-in. Thus only periodically, approximately once or twice a year, the semi-aqueous cleaning bath is discarded and sent off-site as a hazardous waste fuel supplement. In the case of EC-7R, the purchase price of the material includes the cost of disposal as a hazardous waste. Ultimately, based on volumes generated, the EC-7R may be recycled by a hazardous waste vendor.

In the case of the saponified aqueous cleaning sumps, these sumps are generally discharged every eight to sixteen hours of operation and generally average about 100 gallons in size. These wash tank dumps from the saponified aqueous systems contain the majority of heavy metals, flux residues, and extremely high pH and BOD/COD values.

The need for frequent batch dumps on the saponified aqueous cleaning systems results in the use of high quantities of heated water with saponifier and also a large requirement to treat these wash tank dumps prior to discharge. Historically, the reason for short bath life has been that the surfactants, which are volatile, evaporate over time which lowers cleaning effectiveness.

Based on a matrix evaluation of semi-aqueous versus saponified aqueous cleaning, which included health & safety impacts, environmental impacts, cleaning effectiveness and operating costs, the decision was made to pursue the use of the terpene cleaner EC-7R in the Phase II Pilot Facility. The Phase II Pilot Facility, which includes 2 cleaners and 2 closed-loop processors, will be installed in a Raytheon Massachusetts facility for cleaning tests on Raytheon products. Although the Hollis machine cleaned to an acceptable level, it was not incorporated in the pilot facility due to the presence of glycol ethers in the saponifier, projected higher annual operating costs, as a result of frequent wash tank dumps, and a lower potential to allow closed-loop rinsewater processing.

In the area of closed-loop rinsewater processing, the semi-aqueous systems have been designed to readily separate the cleaner from water thus providing an advantage over saponified aqueous systems. Due to the accelerated nature of Raytheon's Alternate Cleaning Technology Program, the decision to move forward with a semi-aqueous cleaner was made in December of 1990. At that time, the technology to close-loop the Axarel-38 product had not yet been defined by Dupont. On the other hand, the EC-7R cleaning compound had been reformulated to enhance its separability from water thus providing an apparent advantage for closed-loop rinsewater processing.

The ACT Phase II Pilot Test Facility which was installed in May of 1991, in one of Raytheon's Massachusetts facilities, included an ECD batch system and a Detrex SA-20 in-line cleaning system, both of which will use the EC-7R cleaning chemistry. To evaluate the feasibility of closed-loop rinsewater processing, Separation Technologists and Simon-WTS systems were installed in the Pilot Test Facility to evaluate their capability in close-looping the rinsewater streams from both the batch and in-line cleaning units. The knowledge gained from evaluating the closed-loop rinsewater processors will also be used to identify appropriate technology that can then be used to polish rinsewaters prior to discharge. This pretreatment will involve removing residual terpene to low enough concentrations to be suitable for discharge to an on-site industrial waste treatment plant or a municipal waste treatment plant.

Both closed-loop processors use phase separation by specific gravity, granular activated carbon for trace terpene removal, ion-exchange particulate filtration and a heating boost back to rinsewater temperature of approximately 100 degrees Fahrenheit.

The quality of deionized water that is required for rinsing of Raytheon CCA's to meet military specifications, ranges between 0.5 and 2.0 megohm. Therefore, the closed-loop processors need to supply deionized water on a continuous basis within that acceptability range.

During the pilot test running of the closed-loop equipment, four significant items of information are needed:

1. Definition of Annual Operation & Maintenance Costs

Using the present technologies, costs are a function of the amount of consumable exchange media (Granular Activated Carbon and Ion-Exchange Resins) that will be used on an annual basis. The life expectancy of the exchange medias is directly proportional to the efficiency of the phase separator units and inversely proportional to the temperature of the rinsewaters. Initially, rinsewater temperatures will be 120 degrees Fahrenheit, however an effort will be made to lower the temperature to 80 degrees Fahrenheit, which will lower operating costs, reduce terpene air emissions and extend exchange media life.

2. Logistics of Closed-Loop Rinsewater Processing

A hydraulic balance needs to be attained between the cleaners and the closed-loop processor. The feasibility of this balance will be determined during the pilot test.

3. Potential to Accumulate Contaminant(s) or Organism Growth in the Closed-Loop System

Due to the lack of a large installed base of closed-loop processors on RMA Flux Cleaners, analytical work will be done on the treated water to determine if any contaminants are accumulating.

In addition, the system will be monitored closely for any signs of microbial growth that may develop. If necessary, a disinfection/sterilization step may need to be added to the system.

4. Treatment Efficiency of the Phase Separators

Depending on the type and quantity of cleaner installations and the facility's capability to discharge wastewater, it may be most practical to treat and discharge rinsewaters. An example would be the installation of 2 batch units, which would not justify the need to close-loop rinsewaters. For that application, a reasonable treatment scheme may be to phase separate the rinsewater and then polish with granular activated carbon prior to discharge. Evaluating the treatment efficiency of the phase separators and granular activated carbon steps will determine the quality of effluent that is achievable.

SUMMARY

Results from the Raytheon ACT Initiative Phase I indicated that the following 4 processes, 3 semi-aqueous and one saponified aqueous, cleaned the Raytheon test board equal to or better than the TCA/DI water/IPA baseline:

In-Line

Detrex SA-20 using Axarel-38
Hollis Hydro-Station 332 using Federated Fry 3555

Batch

ECD 6307/6300 using EC-7R
Accel Microcel II using EC-7R

Based on a matrix which included health & safety, environmental, cleaning effectiveness and operating costs, the decision was made to pursue the use of EC-7R in the Phase II Pilot Test Facility.

The facility will include two cleaning systems, namely, the ECD 6307/6300 and the Detrex SA-20 and 2 closed-loop rinse water processors, one manufactured by Separation Technologists of North Reading, Massachusetts and one unit from Simon-WTS of Santa Clara, California.

Follow-up work also continues with Hollis and Accel. In the case of Hollis, an effort continues to identify a non glycol ether saponifier that will provide effective removal of RMA flux. Accel's Microcel II is being evaluated for application specific opportunities using EC-7R.

The Phase II Pilot Facility was started up in June of 1991 at a Raytheon location in Massachusetts. The process parameters for the effective cleaning of the test boards were reverified, and all Raytheon locations have performed cleaning tests of actual production CCA's at the pilot facility.

The objectives of the Phase II pilot testing program and findings to date are shown below.

Process

- Develop and document a cleaning process that routinely meets military specifications
- Identify bottom-line costs
- Ensure no reliability concerns exist

Testing to date at the pilot facility using a variety of CCA's, including very complex modules that are significant cleaning challenges, have been successfully cleaned to meet military specifications. Line speeds in the Detrex machine using the test board as a baseline have averaged 5 feet per minute, with the rinsewater temperature at machine ambient, which averages approximately 95 degrees Fahrenheit, due to the energy addition of high volume pumps. Cleaning of complex CCA's may require modification of the operating parameters.

Based on operating costs, preliminary calculations rank saponified aqueous cleaning as the most expensive, our 1,1,1 trichloroethane/deionized water/IPA baseline as the second most expensive and the semi-aqueous process using EC-7R, as the least expensive cleaning process.

Material compatibility results on saponified aqueous cleaners revealed problems with metals and metal finishes, such as black anodized aluminum. The EC-7R material was found to have similar effects to that of 1,1,1 trichloroethane; namely silicones and low modulus (soft) polyurethanes being the problem areas. The materials compatibility issues with the terpenes will be manageable.

Customer

- Gain acceptance of alternate cleaning process

Customer acceptance continues to be the greatest hurdle left in our ACT initiative. Specification incompatibility is the single biggest problem hindering the implementation of the alternate cleaning process. Short of a global solution, locations will need to follow the expensive, time consuming contract modification route. Raytheon continues to explore this issue through a variety of avenues.

Environmental

- Closed-loop rinsewater processing
  - Definition of annual operating & maintenance costs
  - Logistics of closed-loop processing
  - Potential to accumulate contaminant(s) or organism growth problems
  - Treatment efficiency of phase separators and granular activated carbon systems

- Development of a detailed material life-cycle for the terpene cleaner, including fugitive and stack air emissions as well as wastewater impacts
- Volume of waste terpene generation

The process of close-looping the rinsewaters in the pilot facility has proven to be very successful. The hydraulic balancing and water quality have been totally acceptable to date. The operation of the pilot facility has been in a zero discharge mode from June to September of 1991. All rinsewater generated from the ECD and Detrex cleaning systems have been effectively treated and returned to the cleaners for reuse. Due to limited loadings of flux and terpene dragout during the duration of the pilot plant operation, we were unable to quantify the life expectancy of the closed-loop rinsewater processors. The units did process over 3500 CCA's without requiring exchange media changes.

Analytical testing of the rinsewaters from the batch and in-line cleaning systems, using Raytheon test boards (4" x 7"), revealed lower than anticipated BOD and COD levels. The ECD batch cleaner composite rinsewater samples averaged less than 300 mg/1 of BOD and COD. It is important to note that the first rinse discharges from the cleaner contain the majority of the contaminants. For example the first rinse (prewash), had a BOD value of 1250 mg/1 and a COD of 8600 mg/1, while the composite of all the rinses together had a BOD of 140 mg/1 and a COD of 275 mg/1. Each rinse discharge in the ECD is 2.5 gallons, with total rinsewater discharges averaging 10 - 15 gallons per batch, based on the number of rinses used. This data was from a run of 30 Raytheon test boards, 15 on each of the upper and lower racks.

The in-line Detrex cleaner rinsewater averaged less than 200 mg/1 of BOD and COD. These results were produced with the conveyor containing test boards over its entire length. The Detrex unit in the pilot facility contains a pumped sump that has resulted in the accumulation of a supernatant layer of terpene. This separation has lowered the terpene burden on the closed-loop rinsewater processors.

Stack sampling has been performed on the Detrex machine and results are pending as of this writing. A definite correlation can be drawn between terpene air emissions and ventilation flows. Proper ventilation control and interlocking can minimize terpene air emissions. Based on results to date, the majority of terpene consumption in an in-line system is via air emissions and not in the form of dragout from the spray-under-immersion cleaning tank.

Health & Safety

- Employee exposures to terpene compounds
- Effectiveness of fire detection and suppression systems in cleaning systems

Successful saponified aqueous cleaners contain glycol ethers, which are suspected reproductive toxins and are SARA reportable. Toxicological studies of terpenes have shown minor relevant adverse health effects to date.

During routine cleaning operations, airborne terpene levels in the work area are extremely low, generally less than 1 ppm. Results are pending on exposures that may be encountered using the ECD batch cleaner.

The combustibility concerns of terpenes are manageable with proper machine design. Controls include carbon dioxide fire suppression systems and the use of nitrogen inerting atmospheres.

James Criscione is an Advanced Manufacturing Engineer at Raytheon. He has had 15 years of experience in electronics assembly, with areas of expertise in surface mount assembly, hybrids, and related materials and processes. He holds a BS degree in Chemical Engineering, as well as an MBA degree, and is the author of several papers.

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EVOLUTION OF SOLDERING SPECIFICATIONS

by
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Paper not available in time to be included in this publication.

REDUCING THE EMISSION OF OZONE DEPLETING CHEMICALS THROUGH USE OF A SELF-CLEANING SOLDERING PROCESS

by

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ABSTRACT

Motorola has joined with Sandia and Los Alamos National Laboratories to perform work under a Cooperative Research and Development Agreement (CRADA) to reduce the use of CFC's and other ozone depleting printed wiring board (PWB) cleaning solvents. This study evaluated the use of a new soldering process that uses dilute adipic acid in lieu of rosin flux. The process consumes the adipic acid in lieu of rosin flux. The process consumes the adipic acid during the soldering process and precludes the need for subsequent cleaning with ozone depleting solvents.

This paper presents results from a series of designed experiments that evaluated PWB cleanliness as a function of various levels of machine control parameters. The study included a comprehensive hardware reliability evaluation, which included environmental conditioning, cleanliness testing, surface chemical analysis, surface insulation resistance testing, along with electrical, mechanical and long term storage testing.

The results of this study indicate that the new process produces quality, reliable hardware over a wide range of processing parameters. Adoption of this process, which eliminates the need for supplemental cleaning, will have a positive impact on many environmental problems, including depletion of the ozone layer.

INTRODUCTION

The destruction of the Earth's protective ozone layer is one of today's larges environmental concerns. Printed wiring board (PWB) cleaning solvent emissions have been identified as a primary contributor to this destruction. Industry has responded to this threat by developing new self-cleaning soldering processes, which eliminate the need for subsequent PWB cleaning. However, these processes have not yet been approved for military hardware applications. This paper describes a task designed to evaluate a new self-cleaning soldering process, and to prove that hardware produced by the process is acceptable for military applications.

The program is a joint effort undertaken by Motorola Inc., along with Sandia and Los Alamos National Laboratories. This work is being accomplished as part of a Cooperative Research and Development Agreement (CRADA) under the Department of Energy (DOE) Industrial Waste Reduction Program (IWRP). The objective was to evaluate the new process, solder hardware thereon, subject the hardware to environmental screening, and perform appropriate reliability testing and analysis. The data from these tests will be used to support approvals of the process for military hardware applications.

The program was approximately 75% complete in early December 1991. This paper describes the events that led to the undertaking of this program; the experimental approach and testing methodologies employed; the results from the experimentation and analysis thereof; and the conclusions based on the results-to-date. Post test analysis and supplemental testing was still in-process, the results therefrom will appear in a final report at the end of the program.

BACKGROUND

The impact of the emission of ozone depleting chemicals (ODC's) on the ozone layer is well documented. It has been estimated that one-fifth of these ODC emissions come from cleaning processes for PWB's and other electronic gear (Reference 1). In response to this environmental problem, industry has started using alternate solvents with lower ozone depletion potentials (ODP's); developed new, non-ozone depleting solvents such as terpenes; installed conservation techniques to reduce the emission of ODC's where alternate solution have not been discovered; and developed self-cleaning soldering processes. Conservation techniques and the use of lower ODP solvents are only short term solutions, as environmental legislation and cooperative efforts, such as the Montreal Protocol, are striving to eliminate all ODC usage by the year 2000.

Alternate cleaning solvents are not the optimal solution, as they still have negative environmental and economic impacts. These negative factors include; 1) the environmental impacts of procuring raw materials for cleaning equipment fabrication; 2) the large amount

of energy consumption for conversion of these raw materials into fabrication materials, cleaning machine fabrication, cleaning solvent production and cleaning equipment operation; 3) the environmental impacts of disposal or reclamation of these alternative solvents; and 4) the economic impact of equipment purchase and operation, and solvent purchase, storage and handling.

There are several self-cleaning soldering processes that have been developed over the past few years. The process utilized in this study uses a dilute adipic acid board preparation solution, coupled with a formic acid vapor in a nitrogen cover blanket in the soldering zone.

Adipic acid is a white crystalline dicarboxylic acid material that is dissolved in anhydrous isopropyl alcohol for use as a flux. The typical concentration of the adipic acid for use as a board preparation material ranges from 1 to 3 percent. Adipic acid has been used as a fluxing material for several years within the commercial electronics industry.

The physical and chemical properties of adipic acid have been evaluated by a number of researchers to characterize the effects of the material after wave soldering (References 2, 3 and 4). The material has been used in commercial electronics assembly for several years, generally in modes that have not used cleaning after wave soldering operations. These applications range from under-hood automotive applications to cellular radio communications.

The adipic acid material used in this study was applied to the PWB's by an ultrasonic spray process. Much of the adipic acid is consumed during the soldering process. At the end of the process only a small percentage of the original amount of material remains on the circuit. During the preheat stage the adipic acid reacts to reduce the tin and lead oxides on the surface of the solder, like normal rosin fluxes. During the preheat period a small amount of the adipic acid is driven off and condenses on the cooler surfaces of the machine. Adipic acid is also driven off during the wave soldering operation.

Formic acid vapor is added to the process by bubbling nitrogen through a liquid formic acid solution. The amount of formic acid vapor introduced to the machine is governed by the nitrogen flow rate. The formic acid in the nitrogen cover blanket acts as an oxygen getter, thereby further reducing oxide formation in the soldering zone. The formic acid decomposes into CO_2 and H_2O due to the heat of the soldering process. An additional benefit of the inert atmosphere is the reduction of dross on the solder pot.

The wave soldering machine used during this program has several key features including three independent conveyors (flux, preheat and solder), a dual wave (turbulent chip and laminar), and an ultrasonic spray head for the board preparation fluid. This soldering process has many controllable parameters which influence visual solder quality and ionic cleanliness. These parameters include:

- flux conveyor speed
- preheat conveyor speed

- solder conveyor speed
- solder pot temperature
- wave angle
- turbulent wave on/off
- adipic acid percentage
- formic/nitrogen flow rate

Motorola uses several of these machines in their commercial divisions with very good success. In addition to improved solder quality, they are seeing improved product reliability. Figure 1 illustrates the reduction in failures observed in accelerated life testing of a commercial product.

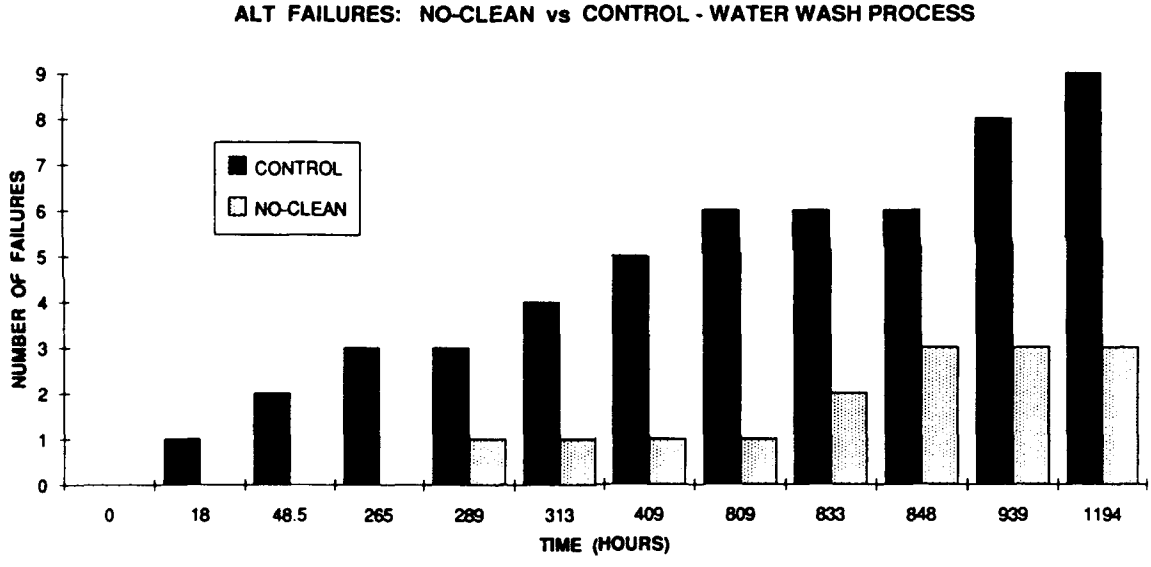

FIGURE 1. Self Cleaning Process Reduces Accelerated Life Test Failures

Military specifications and standards do not allow adipic acid as a fluxing material and mandate that PWB's be cleaned after soldering. Thus, in spite of the successes demonstrated by commercial entities, military contractors are currently prevented from using this new self-cleaning soldering process.

The purpose of the program described in this paper was to evaluate the new self-cleaning soldering process and produce data to show the process produces hardware that is as reliable as hardware solder with existing rosin flux/solvent cleaning processes. This data will be used to support requests for Government approval to use this process in the self-clean mode.

EXPERIMENTS

Recognizing that every different PWB design may have a different combination of soldering parameters to achieve optimal visual solder quality, experiments were performed to define a range of parameters that represented a broad process window. The objective was to understand how the combination of parameters within this window affected solder quality and ionic cleanliness. Hardware was fabricated and tested to demonstrate that any hardware soldered within the process window would be as reliable as the existing rosin flux process.

Specific test objectives were to demonstrate that the process could produce hardware that:

1. Meets the military specification limits for ionic cleanliness and surface insulation resistance;

2. Does not degrade during typical product environmental conditioning; and

3. Does not degrade with long term storage.

The multi-functional Motorola, Sandia and Los Alamos team personnel designed a series of experiments to meet these objectives. These experiments required three different PWB's: a general purpose board, a comb pattern board, and a functional test board. Details of how these boards were used in their respective experiments are described hereafter.

EXPERIMENT 1 – LONG TERM STORAGE VALIDATION

This experiment required a functional board whose performance could be physically measured, and visually inspected, after being subjected to simulated long-term storage testing. An FMU-139 PWB was selected for this purpose.

The FMU-139 is a general purpose bomb fuze, currently being built at a rate in excess of 500 fuzes per day, for Navy and Air Force applications. This is an 0.093 inch thick double-sided board, currently being soldered with a rosin flux/solvent cleaning process.

An initial screening experiment was performed to understand the impact of process parameters on the solder quality and ionic cleanliness of the 0.093 inch thick board. The five soldering process parameters evaluated in the experiment are shown in the following table.

Table 1. Initial Screening Experiment Parameters for 0.093 Inch Thick PWB

Factors	Levels	
	Low	High
Flux conveyor speed	0.8	1.1 meter/min.
Preheat temperature	80	120 deg C
Time in solder pot	3	6 sec.
Adipic acid concentration	1	2 %
Presence of Formic acid	none	7 liter/min.

Please note that the time in the solder pot and preheat temperature are governed by their respective conveyor speeds. The wave angle, solder pot temperature and turbulent wave status were held constant. A half-fraction of a 2^5 factorial experiment was designed, yielding a 16 cell experiment (a cell is a unique combination of process settings). One board per cell was used to gather this preliminary data. The data from this experiment was analyzed using several statistical software packages. The output from these analyses provided information that helped define the soldering parameters for the long term storage test boards.

An analysis of variance (ANOVA) was calculated for those factors influencing visual and cleanliness of the boards after wave soldering. The most significant effects influencing cleanliness and visual defects are reported in the order of their listing:

Cleanliness influence:

Single factor effects:

- Preheat (high level)
- Time on solder pot(high level).

Two factor interaction effects:

- Flux conveyor speed (low level) and preheat (at high level)
- Preheat and adipic acid concentration (both at high level).

Visual defects influence:

Single factor effects:

- Time on solder pot (high level)
- Preheat (high level)
- Adipic acid concentration (high level).

Two factor interaction effects:

- Flux conveyor (low level) and adipic acid (high level)

- Preheat (high level) and adipic acid (high level)
- Time on solder pot (high level) and Formic acid (high level)

On the basis of this analysis, three different parameter combinations (three cells) were selected to produce three sets of boards: one with good solder quality and ionically clean; one ionically dirty (cleanliness $\geq$ 20 $\mu g/in^2$) with marginal solder quality; and one with in-between cleanliness and solder quality. The three factors varied were flux conveyor speed, preheat temperature and time in the solder pot. The adipic acid and formic flow rate were held at the high levels. In addition to soldering three cells in the self-clean mode, a control sample of boards was soldered using the existing optimized rosin flux soldering/solvent cleaning process. Sample boards from each cell, including the rosin boards, were measured in the ionograph.

The FMU-139 Fuze was designed for 10 years of storage. However, the long term storage test was designed to simulate 20 years of storage to examine the process margin. A modified Arrhenius rate equation as shown below was used to calculate the test acceleration factors.

$$\frac{t2}{t1} = EXP\left[\left(\frac{\phi}{K}\right)\left(\frac{1}{T2} - \frac{1}{T1}\right)\right] EXP\left[\beta\left(\frac{1}{RH2} - \frac{1}{RH1}\right)\right] \frac{A\ E_{C2}}{A\ E_{C1}}$$

Where:
- $t2$ = accelerated test time
- $t1$ = simulated time (20 years)
- ϕ = Activation Energy (eV)
- K = Boltzmann's Constant (8.63×10^{-5} eV/°K)
- $T2$ = Accelerated Aging Temperature (°K)
- $T1$ = Normal Temperature (°K)
- β = Humidity Acceleration Constant
- $RH2$ = Accelerated Aging Relative Humidity (%)
- $RH1$ = Normal Relative Humidity (%)
- A = Voltage Acceleration Constant
- E_{C2} = Accelerated Electric Field In Corrosion Region (V)
- E_{C1} = Normal Electric Field In Corrosion Region (V)

Although temperature, humidity and voltages can be used as acceleration factors, only temperature was selected for this test. This is because the product is a one shot device, that sits dormant in an ammo can with desiccant for storage throughout most of its life.

The boards were suspended vertically on a rack, which was placed in a temperature humidity chamber. The boards were subjected to an acceleration temperature of 80 deg C, and a relative humidity of 40% for 2522 hours, which was designed to simulate 20 years of storage. The boards underwent a production line electrical acceptance test at time = 0, 1, 10, 13.3 and 20 years (simulated).

EXPERIMENT 2 – RELIABILITY EVALUATION:

This experiment required a PWB with through-hole components. The boards were subjected to ionograph testing, visual examination, and electrical and mechanical solder joint testing after environmental conditioning. Figure 2 shows a Motorola test board (MTB) that was selected for this experiment. This board contains axial, DIP, and TO-99 components, along with a connector. The MTB was designed to support soldering process optimization studies, and contains numerous features including various hole-to-lead ratios, and different ground plane-to-solder pad combinations.

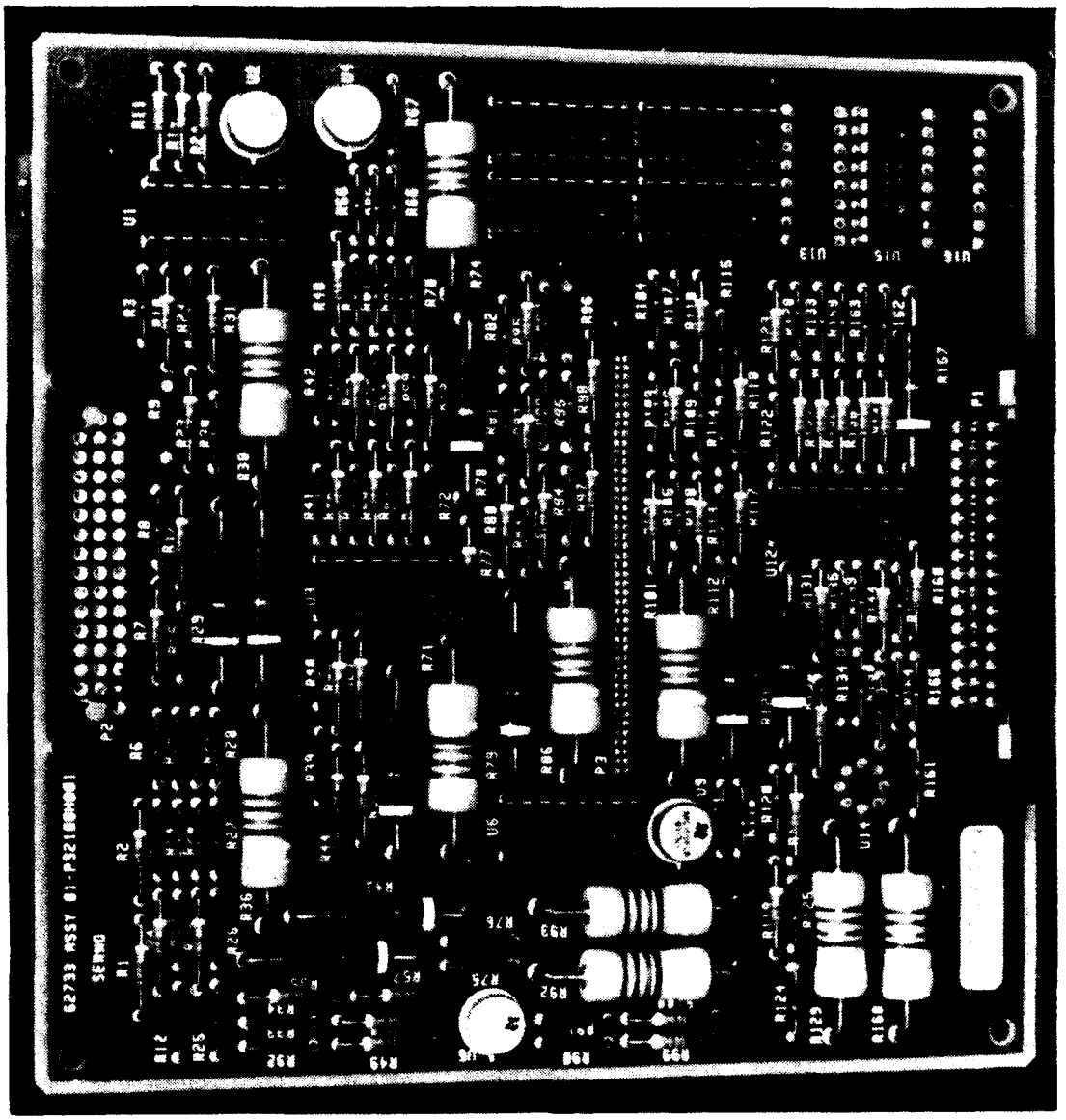

FIGURE 2. Motorola Test Board Used For Reliability Evaluation Testing

An initial screening experiment was performed to understand the impact of process parameters on the solder quality and ionic cleanliness of the 0.062 inch thick MTB PWB. The five soldering process parameters evaluated in the experiment are shown in Table 2. The adipic acid was held constant at 2% and turbulent wave was left on.

Table 2. Initial Screening Experiment Parameters for 0.062 Inch Thick PWB

Factors	Levels	
	Low	High
Flux conveyor speed	0.8	1.2 meter/min.
Preheat temperature	90	130 deg C
Time in solder pot	1.5	4 sec.
Presence of Formic acid	none	7 liter/min.
Wave Angle	5	9 deg
Solder pot temperature	245	260 deg C

A 2^6 full factorial experiment was designed, yielding a 64 cell experiment (a cell is a unique combination of process settings). Two boards per cell were used to gather preliminary data. These boards were visually examined for solder joint quality and had their contaminant levels measured in an ionograph. The data from this experiment were analyzed using several statistical software packages. The output from these analyses provided information that helped define the soldering parameters for the Reliability Evaluation test boards.

An analysis of variance (ANOVA) was calculated for those factors influencing visual and cleanliness of the boards after wave soldering. The most significant effects influencing cleanliness and visual defects are reported in the order of their listing:

Cleanliness influence:

Single factor effects:

- Time on solder pot (high level)
- Preheat (high level)
- Flux conveyor speed (high level)

Two factor interaction effects:

- Flux conveyor speed and preheat (both at high level)
- Preheat and time on solder pot (both at high level).

Visual defects influence:

Single factor effects:

- Formic acid presence (high level)
- Wave angle (high level)

Two factor interaction effects:

- Formic acid (low) and solder temp (high)
- Wave angle (high) and formic acid (either level)
- Preheat (low) and solder temp (high)
- Preheat (low) and formic acid (low)

The flux conveyor speed, preheat temperature and time in the solder pot were selected as the variable parameters for the reliability evaluation test hardware on the basis of the screening experiment. The remaining parameters were fixed at their respective high levels. A lower adipic acid percentage, lower formic acid flow rates, alternate wave angles or solder pot temperatures should not adversely impact board cleanliness. The selected combination of variable and fixed parameters were thought to best define an overall process window that would produce reliable hardware. The statistical analysis of the screening experiment data suggested that a wider range of the selected variable parameters levels should be used. The new levels of the varied parameters are shown in the following table.

Table 3. Reliability Evaluation Experiment Soldering Parameters

Factors	Levels	
	Low	High
Flux conveyor speed	0.7	1.4 meter/min.
Preheat temperature	85	130 deg C
Time in solder pot	1.0	4 sec.

A 2^3 factorial experiment was designed, utilizing the three varied soldering parameters, this yielded an eight cell experiment. An additional set of boards was soldered using the traditional rosin flux process, followed by a solvent cleaning operation. The performance of the self-cleaning process boards was compared to the rosin flux boards throughout all tests. Sample boards from both processes had their ionic cleanliness measured on a Model 500 Ionograph.

An attempt to measure free adipic and formic acid residues on the boards was made using the IPC Honeywell Procedure 355 for HPLC analysis for conventional solder residue

component determinations (e.g., abietic acid, neoabietic acids, Pb and Sn salts of these acids). Although this procedure works well for conventional solder fluxes, the uncomplexed formic and adipic acids are only sparingly soluble in the acetonitrile solvent used for elution. Regardless of this limitation, modifications to the IPC Honeywell 355 procedure were developed that allowed an analytical detection limit of $\cong$40 $\mu g\ cm^{-2}$ for adipic acid to be achieved. An ASTM procedure for hydrocarbon greases and oils was followed for determinations of residual contaminates on an identical set of boards. This procedure entailed washing the solder side of the board with 113 Freon and monitoring the absorbance of the CH stretch region in a long (0.5-2.0 mm) path length liquid IR cell.

A suite of pre and post-mortem surface analytical techniques have also been utilized to examine the state of initial surface cleanliness and corrosion products following long term storage. These methods have included optical microscopy, electron microprobe analysis (EMPA), scanning Auger microscopy (SAM), imaging secondary ion mass spectroscopy (SIMS), and small area Fourier transform infrared spectroscopy (FTIR).

The effects of corrosion on the soldered PWB's and solder joint electrical and mechanical integrity were evaluated by subjecting boards to temperature-humidity and temperature cycle testing. The temperature-humidity testing followed the specification MIL-STD-331B, Table C1-2. The temperature cycling experiment was a custom designed test with a low temperature of –54 deg C, and a high temperature of +71 deg C. The boards were subjected to over 40 cycles, with 2 hour dwell times at temperature extremes, and a 2 hour ramp rate between extremes.

The corrosion evaluation included visual inspection, followed by surface analysis of any noted residues. The PWB's had the electrical resistance measured through five different solder joints per board. The resistance was measured by probing the joint using a four point Kelvin measurement technique. Two probes were placed on the bottom of the joint, and two on the lead on the top side of the joint, and the measured resistance was recorded. Mechanical joint strength was measured by pulling on select component leads and special pull test pins until failure.

Electrical and mechanical parameters were measured before and after environmental conditioning, and on control sample boards.

EXPERIMENT 3 – SURFACE INSULATION RESISTANCE EVALUATION:

The IPC B-24 printed wiring board was used as the test vehicle for surface insulation resistance (SIR) testing. This board was selected over the IPC B-36 board, which has a surface mounted IC thereon. The B-36 was not used because soldering of the IC on the board could introduce another contaminant, even if the board was cleaned after soldering of the part. Figure 3 shows a soldered IPC B-24 board. The unsoldered board is bare copper, except for the gold plated connector fingers.

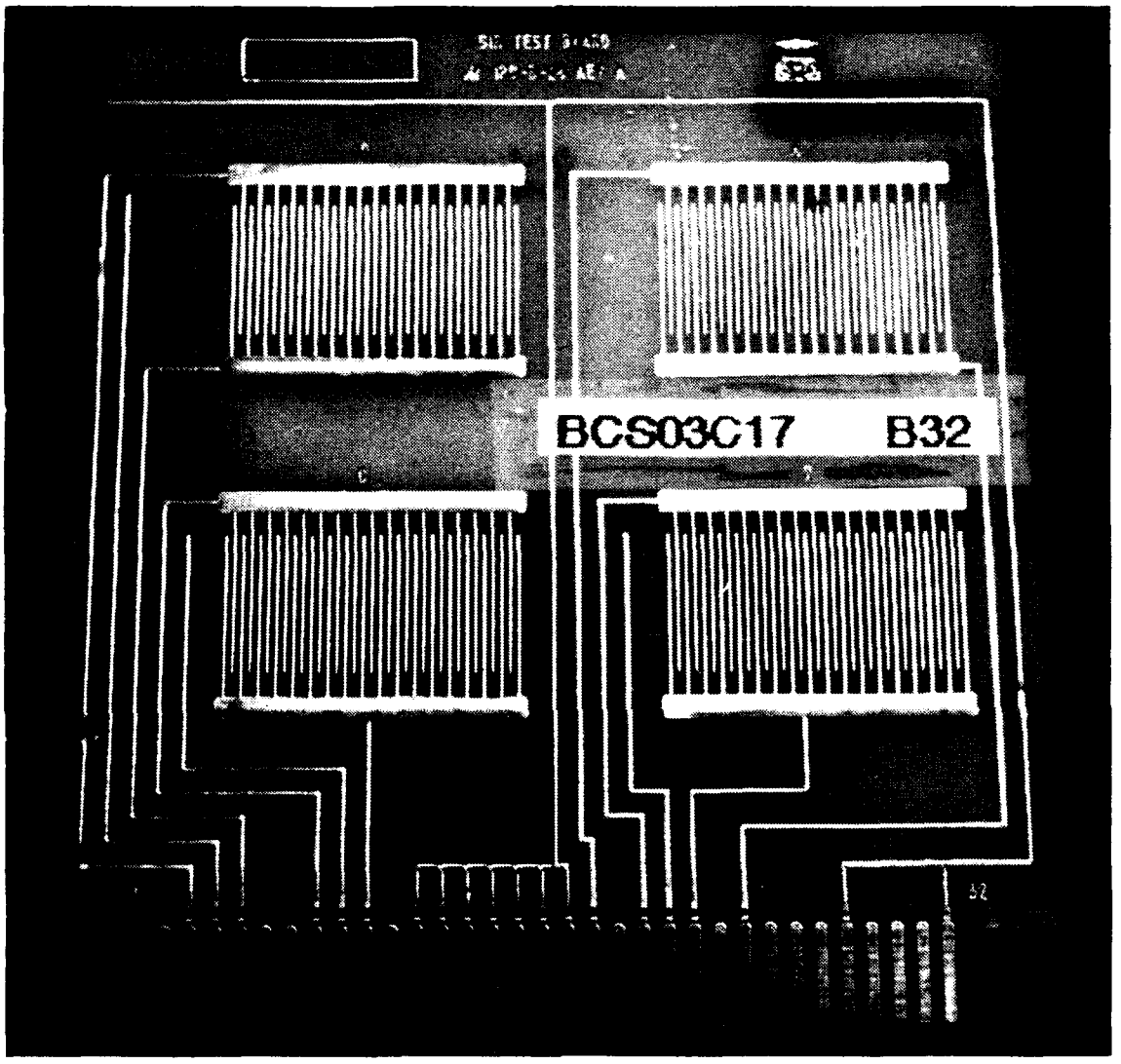

FIGURE 3. IPC B-24 PWB Used For Surface Insulation Resistance Testing

Approximately one-half of the IPC boards were pre-cleaned before soldering, in an effort to remove potential supplier contaminants. The boards were soldered at the same time as the Motorola test boards, with as-received condition and pre-cleaned boards being soldered in each of the eight cells. Similarly, a group of as-received and pre-cleaned boards were soldered with the rosin flux process, followed by a solvent cleaning. In addition, unsoldered PWB's, in the as-received condition were supplied for SIR testing. These boards had PWB supplier contaminants only.

IPC test method 2.6.3.3. defines two different test conditions for SIR testing: 85 deg C, 85% RH; and 50 deg C, 90% RH. The standard test period is 7 days, with measurements at 4 and 7 days being evaluated. Both test conditions were used, with electrical measurements of the board's pattern A being taken at time = 0, 1, 4, 7, 14, and 21 days. Measurements were also taken at time 0 outside of the chamber, and after completion of the testing.

Additional boards were conformal coated and subjected to SIR testing at 65 deg C, 90% RH for 14 days, with measurements at time = 0, 8 hrs, 1, 2, 4, 7, and 14 days. These additional environmental test conditions are defined by MIL-I-46058C, as referenced in Appendix A to MIL-STD-2000A.

RESULTS AND DISCUSSION

The results through early December 1991 have shown that the new self-cleaning soldering process is capable of producing reliable hardware, with visual solder quality equivalent to that achieved with existing soldering systems. Each of the three experiments supported these conclusions with very few anomalies noted.

LONG-TERM STORAGE TEST RESULTS

The long term storage testing compared hardware soldered with the existing rosin flux/solvent cleaning process to the new self-cleaning soldering process over a simulated 20 years of storage. Three different combinations of soldering parameters were used for the new process, in an effort to demonstrate that acceptable hardware reliability could be obtained when processed over a wide range of soldering conditions. Cell 1 PWB's had a solder visual quality similar to that experienced in production, and an average ionic cleanliness of 3.9 micrograms per square inch, as measured on an ionograph. Cell 2 PWB's had an average cleanliness of 3.7 micrograms per square inch and marginal solder quality. Cell 3 was deliberately soldered with conditions known to produce higher ionic contamination levels, and averaged 27 micrograms per square inch. This level is in excess on the MIL-STD-2000A ionograph machine acceptance limit.

Ten PWB's from each cell, and 10 rosin flux soldered boards, were functionally tested periodically during the long term storage testing. All 40 boards passed a production line electrical function acceptance test after t= 0, 1, 10 and 13.3 years (note: the product was designed for a 10-year shelf life). However after 20 years of simulated storage (2522 hours), three units had electrical performance anomalies.

The units with electrical anomalies were visually examined and found to exhibit physical damage to a particular type of ceramic body diode, and localized residue on the board. The remaining boards were examined, and a few were found to exhibit similar visual anomalies, despite being fully electrically functional. Figure 4A shows a damaged diode on

a board from cell 1, which failed the electrical function test in one mode. Figure 4B shows similar damage to the same diode on a board soldered with rosin flux, followed by a solvent cleaning process. Figure 4C shows an undamaged diode of the same type. The diode damage phenomena appeared to be independent of the soldering conditions.

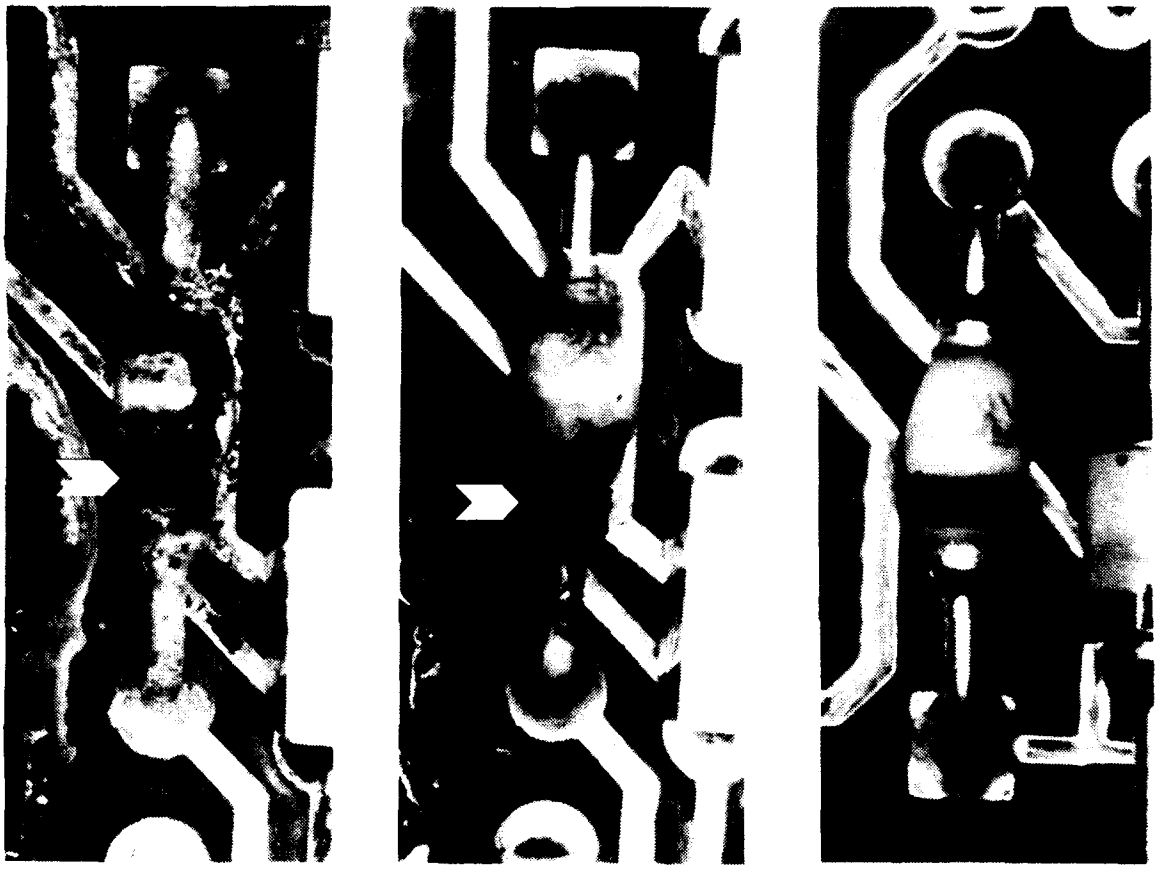

FIGURE 4. Eroded Diode Phenomena Was Also Observed On Rosin Flux soldered Boards A) Self Cleaning Soldering Process; B) Rosin Flux/Solvent Cleaned Process; C) Undamaged Diode

The residue on the board shown in Figure 4A appears to have run down the right side of the board. It appears that water dripped on the board when it was suspended vertically in the environmental chamber. A subsequent examination of the chamber revealed that water condensed on the sides and inside ceiling, and water was dripping down one side. The chamber was disassembled and found to have a bad float in its steam generator. It is suspected that the float failed sometime between 13.3 and 20 simulated years. If so, this would increase the chamber humidity and could cause water to drip along the edge of some of the boards. These conditions would dramatically change the environmental stress on the test samples.

The damaged diodes and residues are being subjected to a post test analysis to verify the suspected cause of the failures. This analysis will not be completed until early 1992, and therefore is not discussed in this paper.

Two extra boards from each cell, and two rosin flux soldered boards were conformal coated and subjected to 14 days of 65 C and 90% RH conditioning. No visual damage to the suspect diodes was noted, and no visible residues were observed.

RELIABILITY EVALUATION TESTING RESULTS

The Motorola test boards (MTB's) were soldered under eight different soldering parameter conditions. None of these boards exhibited any significant problems during subsequent evaluation testing. Figure 5 shows the average results from ionograph testing of five boards per cell, along with five rosin flux soldered boards. An average of 24.5 µg/in^2 for cell 1 boards exceeds the MIL-STD-2000A ionograph machine acceptance limit of 20 micrograms/in^2.

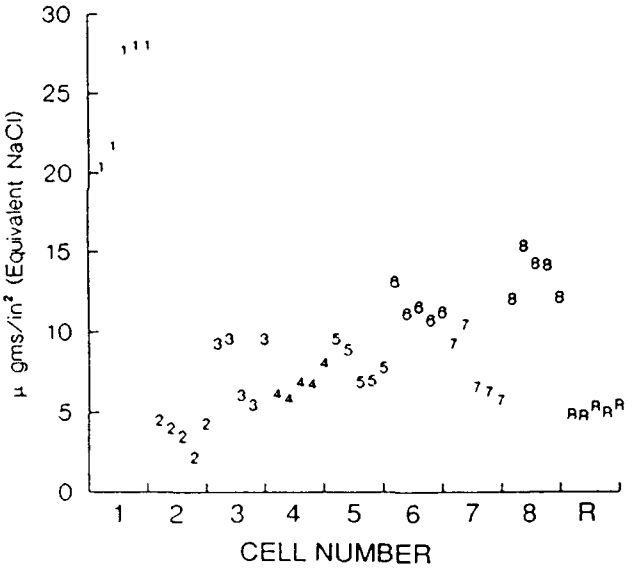

FIGURE 5. Ionic Cleanliness Was Function of Machine Soldering Parameters

Additional ionograph testing was performed by the Navy's EMPF facility in Indianapolis. They used an Ionograph Model 500 SM which employs a heated solution, and therefore should remove more contaminants. Table 4 compares their average results, per cell, to those ionographed at Motorola.

Table 4. Comparison of Motorola and EMPF Ionograph Readings

	ROSIN	1	2	3	4	5	6	7	8
MOTOROLA	5.12	24.45	3.7	8.02	6.78	8.04	11.60	7.7	13.64
EMPF	3.53	30.91	4.52	7.55	6.97	7.94	11.04	7.95	8.24

NOTES: Motorola used Ionograph Model 500
EMPF used Ionograph Model 500SM (heated solution)
Values are cell averages

Several MTB boards were set aside prior to environmental conditioning for analytical determinations for uncomplexed adipic and formic acid residues. All of the test boards examined showed that free adipic acid determinations were below detection limits (40 $\mu g/cm^2$) for HPLC testing. Additional boards were set aside for total residual hydrocarbon content. Free hydrocarbon contamination was barely detected (<2 $\mu g/cm^2$), on only 2 boards. It should be pointed out that the rosin flux soldered boards underwent a solvent cleaning after soldering, and that free formic and adipic acids are insoluble in the 113 Freon eluant used in this testing. Further tests using more appropriate elution solvents were in-process, in December 1991.

Figure 6 shows portions of the MTB boards that were soldered with rosin flux and with the self cleaning soldering process. Figure 6A shows a rosin flux soldered board at 7X, and Figure 6B the same board at 20X. Figures 6C and D show corresponding locations on a board soldered with the new process. The rosin flux soldered/solvent cleaned boards possess bright, clean solder joints, as expected using a well refined technology. The boards soldered with the new process exhibit some white deposits at the base of the solder joints, and in certain depressed regions of the PWB itself. Small area FTIR examination identified the presence of very low levels of adipic and formic acids in certain regions of a few boards. In other regions, the presence of very low levels of partially decomposed adipic and formic acids, and residues from the respective acids, have been spatially imaged using small area reflectance FTIR and SIMS.

FTIR analysis was also performed by the Electronics Packaging Technology Branch of the Product Assurance Division, at the Naval Weapons Center at China Lake California. They concluded that there appeared to be no significant residues, and that the little or no contamination is very encouraging.

Additional boards from each cell, and rosin flux soldered boards, were subjected to temperature-humidity or temperature cycling conditioning, in an effort to evaluate potential corrosion or internal solder joint integrity problems. A subsequent visual examination showed no copper corrosion, and limited amounts of residues as previously discussed. These boards were also subjected to electrical and mechanical testing.

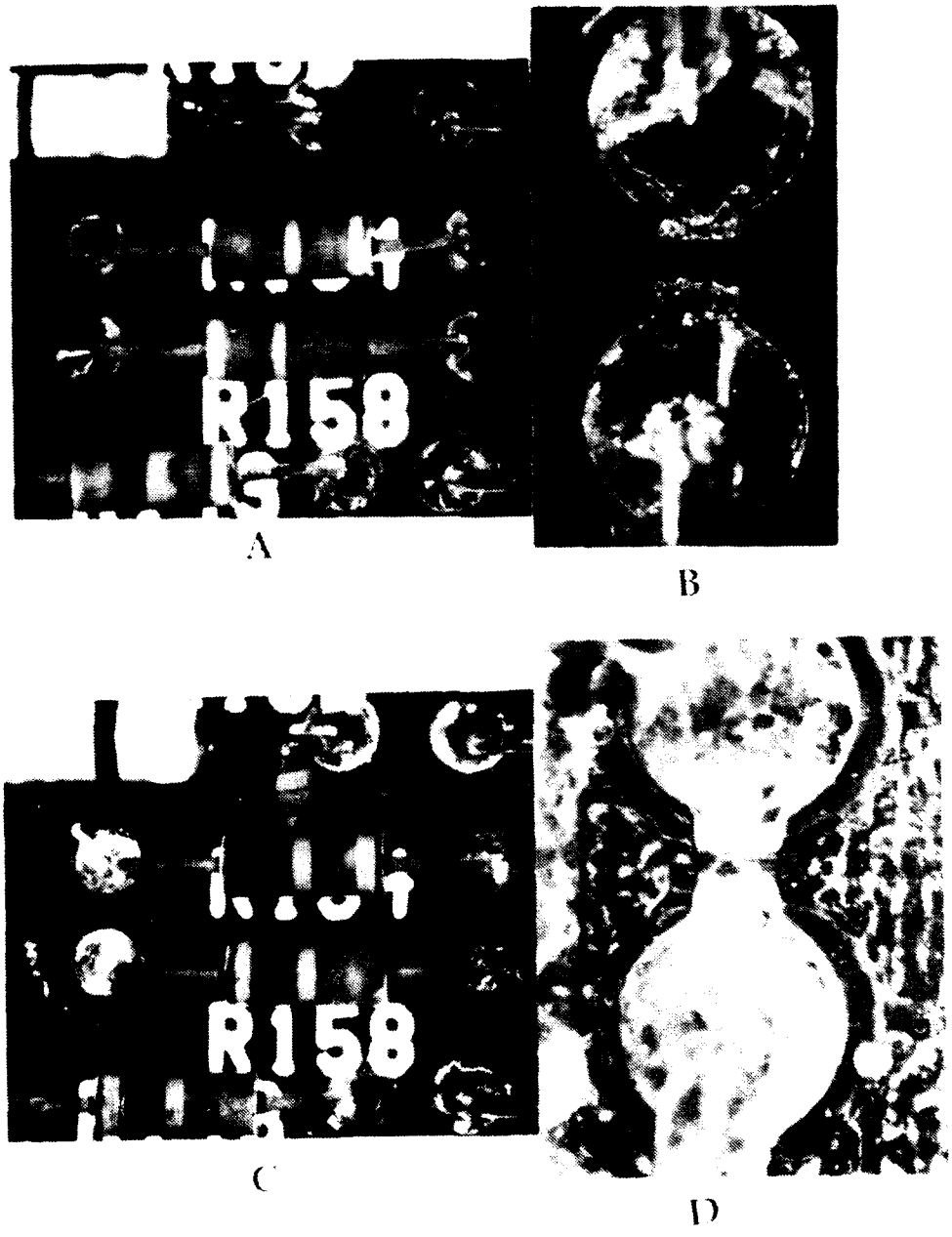

FIGURE 6. Small Amounts of Residues Were Noted on Some Boards

The electrical testing of internal solder joint resistances before and after environmental conditioning differed by less than 250 micro-ohms. There appeared to be no significant difference between boards soldered with the new adipic/formic acid process or the existing rosin flux process. Also, there appeared to be no significant differences between boards subjected to the temperature-humidity and those subjected to temperature cycle testing, or the control sample boards which had no conditioning.

The same boards were subjected to mechanical pull tests, which were designed to verify solder joint mechanical integrity. Component leads and specially designed pull test pins were pulled with all failures coming at greater than 40 pounds.

SURFACE INSULATION RESISTANCE TEST RESULTS

A total of 128 IPC B-24 boards were subjected to SIR testing, with only six boards having low SIR values after 4 and/or 7 days of testing. These boards and their respective test conditions are shown below. The average ionograph readings for MTB's, soldered under the same conditions, is provided as a reference.

Table 5. Select Parameters for Low SIR Value Boards

Cell No.	Pre-solder Status	Envir. condition	MTB cell ave. ionograph
cell 5	pre-cleaned	85 deg C, 85% RH	8.04
cell 8	as-received	85 deg C, 85% RH	13.64
cell 3	pre-cleaned	50 deg C, 90% RH	8.02
cell 8	pre-cleaned	50 deg C, 90% RH	13.64
rosin	pre-cleaned	50 deg C, 90% RH	5.12
cell 1	as-received	50 deg C, 90% RH	24.45

Overall, the SIR values look good, except for the few "bad apples" listed above. Figure 7 shows SIR values, by cell, for pre-cleaned boards, tested in a 50 deg C and 90%RH chamber, for measurements taken on day seven. Notice how the other boards in cells 3,5 and rosin are significantly higher than the their corresponding low readings. It appears the low board readings are independent of the soldering process or parameter levels. These low value boards are being subjected to post test analysis, which should be complete in early 1992. Despite a few low individual values, the average within any cell was in excess of the MIL-SPEC limit of 100 meg-ohms. Cell 1 had the lowest average, which was 105 meg-ohms.

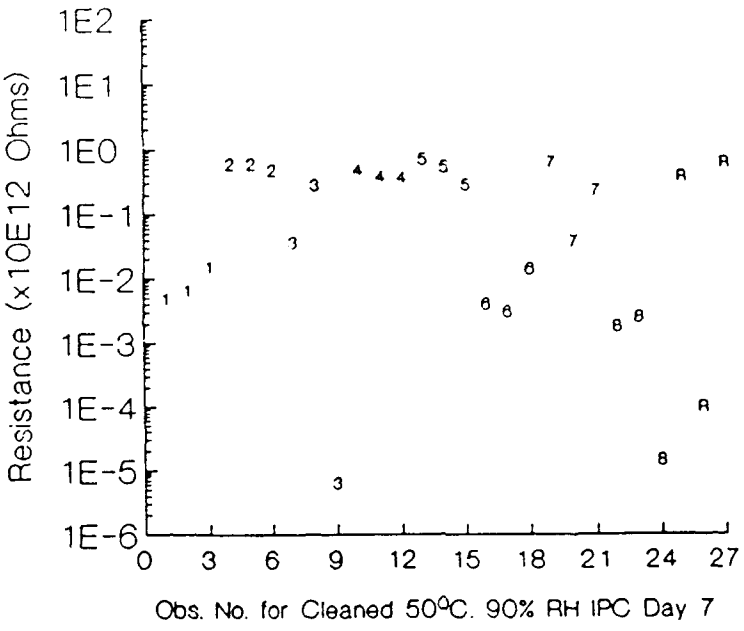

FIGURE 7. SIR Values Looked Good, Except for a Few Bad Apples

Figure 8 is a composite photo of the cell 1, low SIR value board. Figure 8A is an optical image of three of the fingers comprising the test comb pattern. The region outlined in Figure 8A was further examined using EMPA and SAM. The secondary electron image is shown with X-ray maps of Pb, Sn, and Br. Other elements were also analyzed, but were omitted for brevity. The data indicate that this portion of the board grew corrosion residue (10-50 microns thick), over the 21 days of the test (a factor of three over the required seven day test). This residue was determined to be primarily Pb and Sn oxides, intermixed with low levels (<2 wt. %) of Cl, S, and F. The residue is evident in nearly all of the SIR boards with low values.

Figure 9 shows the relationship between cell average ionograph readings and the cell average SIR values. These boards were soldered in the as-received condition, and were subjected to the 50 deg C, 90% RH testing condition. The SIR values were taken on day seven.

MIL-STD-2000A, Appendix A has a test method for qualifying alternate fluxes. Additional boards were conformal coated and subjected to the appropriate test conditions. There were no low SIR values in this group. Figure 10 shows the relationship between cell average SIR values and the temperature/humidity test conditions, on day four. The temperature of the test chamber appeared to have an impact on test values.

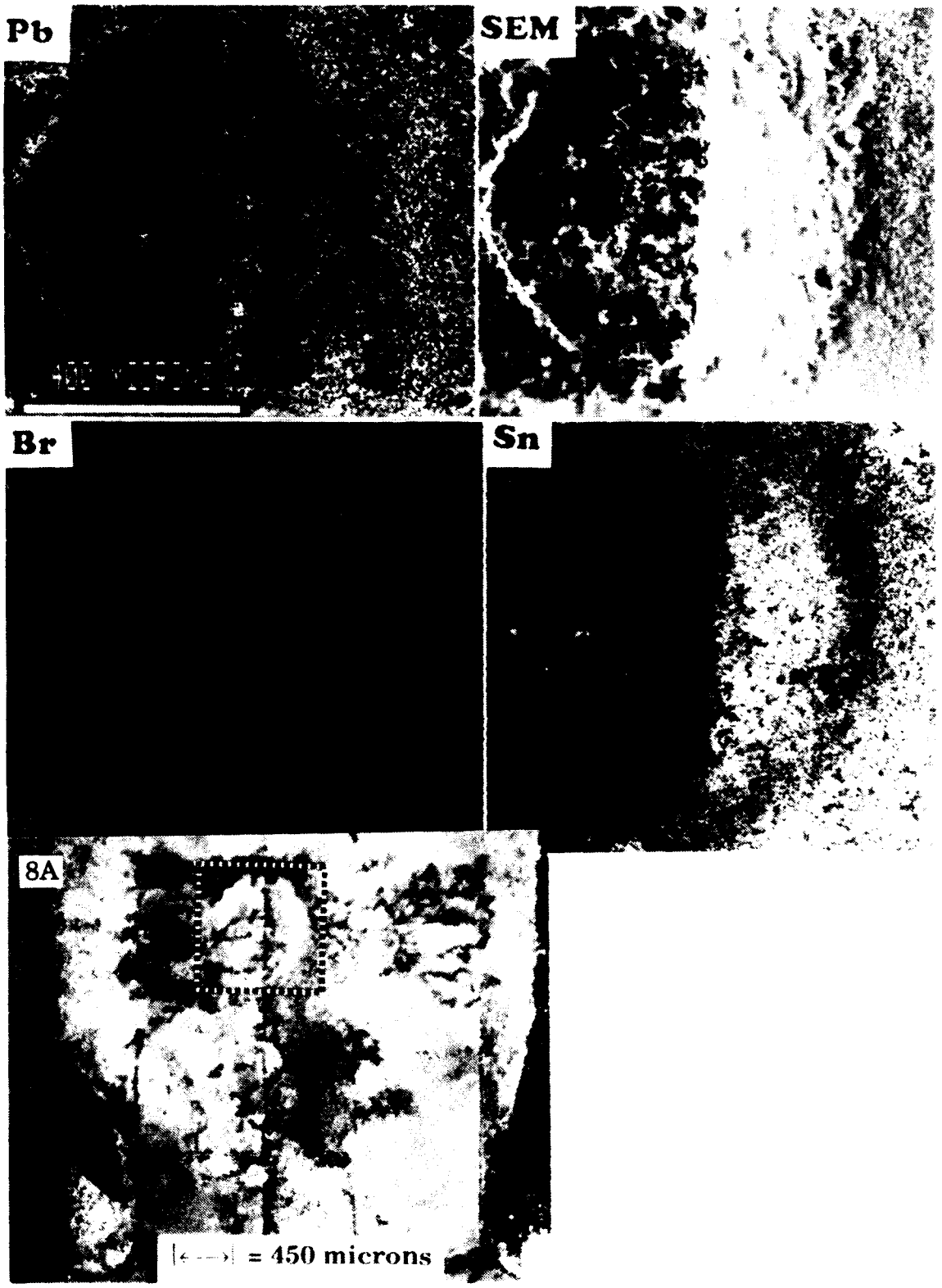

FIGURE 8. Primary Constituents of the Corrosion Spot Have Been Identified

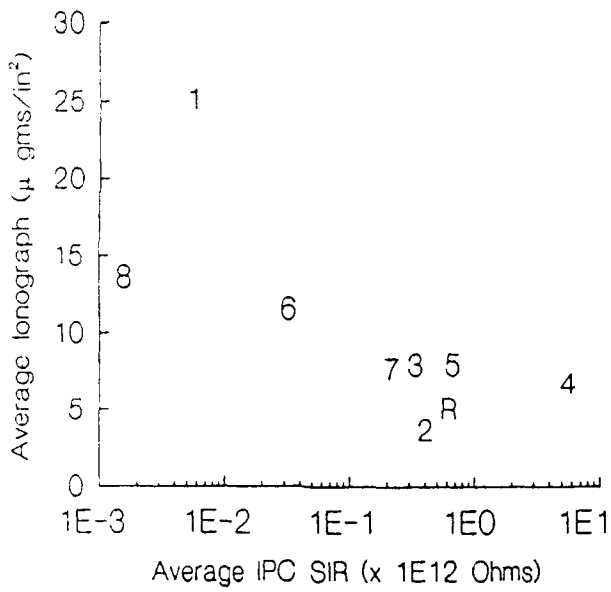

FIGURE 9. Higher Ionic Conductivity Tends to Reduce Surface Insulation Resistance

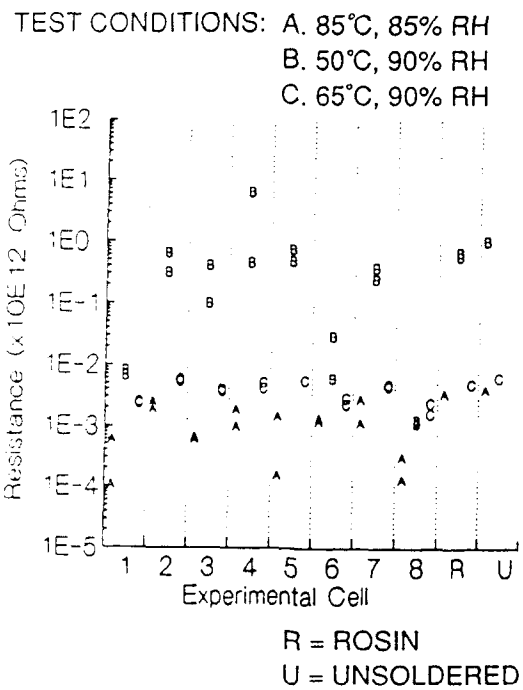

FIGURE 10. Test Temperatures Appear to Have a Larger Impact Upon Sir Values than Conformal Coating

CONCLUSIONS

The test results and analyses through early December 1991 indicate the self-cleaning soldering process will produce reliable hardware. The testing methodologies employed on this program proved sound, with testing parameters generally in excess of specification requirements. The response variables were measured in many ways beyond the usual ionograph and SIR testing. Long term storage, electrical, mechanical and surface analysis testing contributed to verifying the reliability of hardware soldered with the self-cleaning process.

Numerous conclusions were based upon this program's results, including:

1. Visual solder quality equivalent to the existing, optimized rosin flux soldering process could be achieved with the new self-cleaning soldering process. Additionally, the extra control features of the new process offer the potential of better results when the process is optimized.
2. The process produced reliable hardware over a wide range of process parameters. Boards with ionic cleanliness values in excess of the Military Specification limits still proved to be reliable.
3. Minimal residues were observed on hardware, and were judged to have no impact on hardware reliability.
4. Pre-cleaning of PWB's, prior to soldering, generally led to lower initial SIR values.
5. The new process will not degrade product shelf life.
6. The chemistry of the adipic acid solution is straight forward, consisting of a simple formulation of adipic acid and isopropyl alcohol. This provides a consistent material from lot-to-lot, with excellent reproducibility in properties. The advantage to the user is the elimination of dependency upon the addition of other activating agents typical of rosin fluxes.

In summary, this new self-cleaning soldering process appears capable of producing quality, reliable hardware, over a wide range of processing parameters. Adoption of this new process, which eliminates the need for supplemental cleaning, will have a positive impact on many current environmental problems, including depletion of the ozone layer.

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John Fischer and personnel at the Product Assurance Division of the Naval Weapons Center at China Lake California contributed to our planning of the program and contributed to its performance with FTIR testing of sample hardware. Bill Vuono and personnel from the Navy's EMPF facility at Indianapolis assisted by performing ionograph testing on sample boards.

The authors would also like to recognize individuals within their organizations that made significant contributions to the program. These people include J. Doug Farr and W. B. Hutchinson of Los Alamos National Laboratory; Maria Armendariz, Dennis Huffman and Dennis Anderson of Sandia National Laboratories at Albuquerque; and Gene Martinez, Kelly Power, Susan Gray, Donna Combs and Kelley Carleno from the Tactical Electronics Division of Motorola's Government Electronics Group.

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NO CLEAN SOLDER PASTE FOR MILITARY APPLICATIONS

by

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ABSTRACT

Ozone depleting solvents will soon be a thing of the past. New alternatives are aggressively being sought to take their place. Some of the alternatives include no clean fluxes, water soluble fluxes in conjunction with aqueous cleaning, and semi-aqueous cleaning. Each comes with its own share of advantages and disadvantages. Selection requires that consideration be given to each of the viable candidates as determined by product performance and customer specific needs. After extensive testing, Raytheon Company has selected semi-aqueous cleaning as its primary replacement for ozone depleting solvents in cleaning printed wiring assemblies. At Submarine Signal Division, a study was undertaken to further explore no clean solder paste as a complimentary alternative to semi-aqueous cleaning for those applications in which cleaning may be limited by product design. No clean fluxes were selected over water soluble fluxes due to the corrosive nature of water soluble fluxes and the potential risk of incomplete residue removal.

NO CLEAN FLUXES

INTRODUCTION

Through a company wide initiative, semi-aqueous cleaning was found to be the best alternate cleaning replacement for ozone depleting solvents used in the cleaning of printed wiring assemblies. It provides comparable cleaning performance for a majority of printed wiring assembly designs. At Submarine Signal Division we are confronted with several designs which push the limits of existing cleaning systems. Ceramic circuit cards are assembled with surface mount components (leadless chip carriers) which together provide more of a cleaning challenge than that found with conventional printed wiring board assemblies. As such, assemblies must be sent through large inline cleaners a multiple of times to guarantee cleanliness. Semi-aqueous cleaning of these assemblies was an unknown. Further, future designs of increasing cleaning difficulty were anticipated. It was decided that the no clean solder paste option be explored as a potential backup position to future cleaning challenges.

As it turns out, semi-aqueous cleaning can clean these difficult types of assemblies, but only after many repetitive cleaning cycles. Future designs of increasing cleaning difficulty may cause this type of repetitive cleaning to become impractical. Future options available to us include design trade-offs, future cleaning equipment improvements, or the allowance of no clean fluxes. In preparation for this latter option, a feasibility study was initiated. Although still under investigation, some interesting observations have been made.

NO CLEAN SOLDER PASTE

Definitions

Industry Consensus. No clean solder paste typically involves low solids flux whose minimal post reflow solder residue is not detrimental to product reliability for the life of the product within its service environment. Furthermore, no clean flux allows for post solder testing through "bed of nails" fixturing.

Current Study/Evaluation. For the purposes of this study, no clean solder paste follows the above industry consensus with the exception that "bed of nails" fixturing is no longer an issue. Instead, visible flux residue must be removable when cleaned in an environmentally friendly cleaner. This is necessary in order that conformal coating can be applied over residue free surfaces. Flux residue which is entrapped and hidden from view would be acceptable, although not preferred. This would ensure the reliability of those designs which compromise the complete removal of flux residue. This would remove the question of acceptable assembly cleanliness for those difficult designs which currently, erroneously, rely on ionic resistivity testing. (Entrapped flux residues which have avoided removal during cleaning tend to go undetected by ionic resistivity testing which is itself a mild form of wettable surface cleaning.)

Requirements

Given the current study definition, the following requirements warrant evaluation:

1) No clean solder pastes must provide equivalent processing performance.

2) No clean solder pastes must provide equivalent soldering performance.

3) No clean flux residues should be both minimal and cosmetically acceptable.

4) No clean flux residue must not compromise product reliability.

5) No clean flux must be removable through cleaning.

6) No clean flux residue must not negatively effect conformal coat performance.

Phase I Testing

At the time of this writing, Phase I testing has been completed. This testing involved the evaluation of thirteen different no clean solder paste samples as provided by ten different suppliers. The purpose of this phase of the evaluation was to determine whether no clean solder pastes could perform as well as current baseline solder paste. If so, downselection from the field of thirteen samples to a more select few would be made for the second and final phase of the evaluation.

Phase I involved basic comparison testing. (Reference Table 1.) Upon opening sample jars, paste condition, as a result of short term storage, was examined. High viscosity samples were noted and compared to their original manufacured viscosities. It was found that of the three high viscosity samples, one was formulated to be high (sample 1), another (sample 5) performed poorly, and the third was determined to require storage under refrigeration (sample 6). A second paste condition which was examined was flux retention during heating. Samples in which flux spread during initial heating were so noted.

Soldering performance was determined using two types of tests. Each type was performed under three different reflow conditions: vapor phase, infrared in an air atmosphere, and infrared in an inert nitrogen atmosphere. The first test evaluated the adhesive forces of the solder paste and involved the degree of solder spread average diameter onto a copper coupon. The numbers in Table 1 (identified under solder wetting) are actual physical measurements of the solder spread onto the coupon, measured in mils. The larger the spread, the better the solder wetting. The second test involved the cohesive force of the solder paste as determined by the number of solder balls generated when solder paste was printed onto a non solderable surface. The numbers in Table 1 (identified under solder balls) represents the actual count.

The final comparison involved a ranking of visible flux residue based upon quantity, spread, discoloration, and overall cosmetic condition. A ranking of 1 indicates little residue, whereas a ranking of 4 indicates significant residue. (Reference Table 1.)

The results of Phase I testing, as indicated by Table 1, are very encouraging. Five of the thirteen samples performed comparably to that of the baseline. Samples 1 and 9 exhibited equivalent wetting performance to that of the baseline, with an overall reduction in solder ball count. Samples 3, 6, and 7 exhibited good solder performance with notable reductions in visible flux residue. It was also evident that infrared heating in an inert nitrogen atmosphere is the preferred method of reflow.

Phase II Testing

Based upon Phase I testing, five candidate materials have been selected for Phase II testing. Phase II testing is designed to determine the feasibility of allowing entrapped, hidden flux residue to remain upon a finished assembly. It will also determine the processibility of the new solder paste systems. Phase II evaluations include surface insulation resistance, ionic resistivity, corrosivity, conformal coat compatibility, cleanability (using semi-aqueous cleaning), printability, printing life, and tack life. Omitted from this testing are pH titration, halides (silver chromate paper test), and electromigration. pH and halide testing are best suited to material lot qualification by the solder paste supplier. Electromigration testing can be used in material qualification of solder masks.

Surface Insulation Resistance. Surface insulation resistance between adjacent solder terminations will be measured for both 0.050 in. and 0.025 in. pitch leadless chip carriers on uncleaned samples. This would represent the worst case of flux entrapment beneath a leadless chip carrier. This is different than the typical test utilizing comb patterns beneath devices which measures cleaning performance.

Ionic Resistivity. This test will determine the ionic activity of the flux residue following reflow. Again, cleaning will not be performed prior to testing.

Corrosivity. This testing will be performed both for corrosion of the raw flux (copper mirror test) as well as for corrosion of the flux residue following reflow (copper coupon test).

Conformal Coat Compatibility. Conformal coat will be applied directly over flux residue to determine the need for visible flux residue removal. Coupons will be subjected to thermal conditioning and to humidity testing.

Cleanability. Flux residue will be removed using semi-aqueous cleaning to ensure compatibility.

Solder Paste Processing. Printability, print definition, print life (length of time solder paste can be used during printing), and tack life (time allowance for component placement) will be evaluated. No clean fluxes tend to have short storage and working lives due to reduced flux content.

SUMMARY AND CONCLUSIONS

Results to date suggest that no clean solder paste in conjunction with semi-aqueous cleaning may provide a satisfactory means by which to ensure the reliability requirements of difficult-to-clean assemblies. This approach may better assure the quality of an assembly than can questionable ionic resistivity testing of difficult-to-clean assemblies. Acceptance of no cleans could eliminate the need for this test.

TABLE 1
PHASE I TESTING RESULTS OF THIRTEEN SOLDER PASTES

SAMPLE	PASTE CONDITION	SOLDER WETTING V	A	N	SOLDER BALLS V	A	N	FLUX RESIDUE
1	1+	178	172	180	10	22	6	4
2		170	172	<174>	10	19	17	4
3		172	174	174	12	20	9	3
4		<176>	168	172	24	10	15	4
5	1+	146	*	*	7	@	15	1
6	1+	158	174	172	40+	#	10	1
7		170	172	172	4	#	4	2
8		<172>	172	172	12	#	8	4
9	$	174	172	178	13	5	8	4
10	$	166	168	168	14	4	9	4
11	$	154	162	166	29	10	2	4
12		162	170	170	28	26	4	3
13		168	168	168	11	5	5	2
SMPL AVE		166	170	172				
BASELINE CONTROL		180	178	178	15	4	17	4

NOTES:

1+	=	viscosity exceeding 1 million cps
40+	=	more than 40 solder balls
*	=	gross dewetting & nonwetting
#	=	many solder fines
@	=	gross dewetting
V	=	vapor phase soldered
A	=	IR reflowed in air
N	=	IR reflowed in nitrogen
1-4	=	flux residue rating, where 1 is little residue and 4 is significant residue
$	=	flux spread during heating
< >	=	solder splatter

- Solder wetting numbers are a measure of average diameter, in mils.
- Solder ball numbers are a count of solder balls (excluding fines).

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A NEW CHEMICAL CLEANER FOR THE ELECTRONICS INDUSTRY

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ABSTRACT

A careful analysis of the chemical nature of the common contaminants requiring removal from printed circuit assemblies has been undertaken. This, combined with an investigation of the physical requirements for cleaning circuit assemblies, has resulted in the development of a new cleaner coded Formulation SL9. Throughout the development of Formulation SL9 the need to minimise its environmental impact has been a primary concern. The resultant cleaner combines solvency power with the necessary polarity to enable it to remove both rosin and ionic activator residues without the need for aqueous rinsing. Analysis of pcbs cleaned with this type of solvent have shown that it achieves levels of cleanliness better than those required by Military Specifications.

The ability to use the same fluid to both clean and rinse pcbs provides for simplicity of use. For example, a simple 4 stage cleaning process consisting of wash - rinse - polish and drying cycles provides effective cleaning to the most stringent standards. Cleanliness of the final rinse stage can be ensured by re-circulating the solvent through a series of quality control packs which remove any trace of contamination.

INTRODUCTION

The need to eliminate the use of environmentally unacceptable CFCs for cleaning circuit assemblies has presented the electronics industry with a major problem. Current international agreements call for the phase out of CFCs by the year 2000, many countries have already introduced legislation to phase out these materials even more rapidly. The need for a replacement is increasingly urgent.

By dividing the solvency characteristics of a molecule into dispersive, polar, and hydrogen bonding forces, and assuming that like dissolves like, potential solvents for specific resins can be identified. In the case of flux residues the situation is complicated by the presence of chemically very different activators and rosin residues. While it is relatively easy to identify materials which will remove either rosin or activators, it is much more difficult to identify a single material which removes both effectively. It's necessary therefore to develop a blend of miscible solvents (in a similar way to current CFC cleaners).

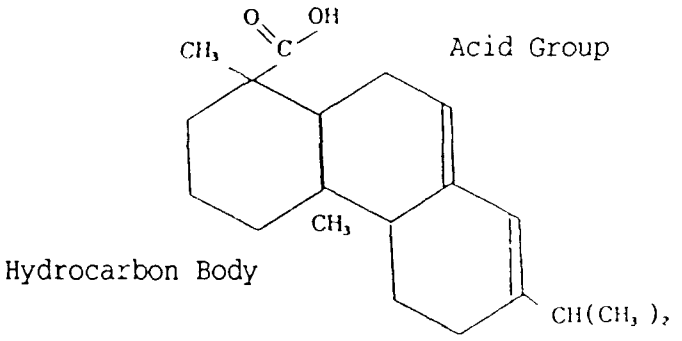
Other key properties identified as being essential in an alternative are related to the process, handling, and transportation of the material. The aim of this project was to develop a product that was simple to use, cheap to store and easy to transport. Since the product is for an environmentally sensitive application the environmental impact of the material was a top priority. Two approaches have been used here, one is to use only materials with low environmental impact , and the other is to use materials in equipment which minimise emissions to the environment. Best results are achieved when the material is used in specially designed equipment. The ability to the same fluid in both the wash and rinse allows the use of a simple 3 or 4 stage cleaning process.

FLUX REMOVAL

The solvent characteristics of a molecule can be described by the types of interaction taking place between the molecules. These interactions can be divided into three types; dispersive forces, polar forces, and hydrogen bonding forces. In the case of hydrocarbon materials there are only dispersive forces present. The introduction of hetro-atoms (e.g. oxygen, chlorine, nitrogen) will introduce polarity and in some cases hydrogen bonding. The exact nature and extent of the polarity and hydrogen bonding present in a molecule is dependent on the number of hetro-atoms, their position in the molecule and the functional group they are in (e.g. alcohol, ether, ketone etc.). In this work oxygen is the hetro-atom. Even with this limitation it is possible to produce compounds with properties that span from oleophilic (hydrocarbon like) to hydrophilic (water like).

Analysis of natural rosin shows it to be a complex and variable mixture of materials. The major constituent of which is abietic acid(see fig 1). Although it is an acid the majority of the molecule is however hydrocarbon in nature. It is this part of the molecule which dominates its solute characteristics. Hence the efficiency of hydrocarbon cleaners already available to the market. However these compounds are very poor at removing ionic materials which are highly polar in nature, hence the need for the water rinses. If water and hydrocarbons were miscible then by mixing them together it would be possible to produce a single fluid which removed both ionic and rosin residues. By using oxygenated solvents it is possible to have oleophilic and hydrophilic materials which are miscible and consequently have a single fluid that removes both types of residue.

FIGURE 1 Chemical Structure of Abietic Acid



Having identified the required solvent characteristics for removal of rosin and activator residues a number of formulations were prepared using miscible materials. These were subsequently tested for efficacy using a range of fluxes on test boards, At this stage a simple room temperature immersion wash followed by a single rinse was used. From this work the best formulations were selected and an optimisation exercise carried out. This resulted in a number of formulations, which were all similarly effective. To differentiate these a further set of operating requirements were applied which resulted in the selection of a single optimum fluid with a laboratory code formulation SL9.

OPERATING REQUIREMENTS

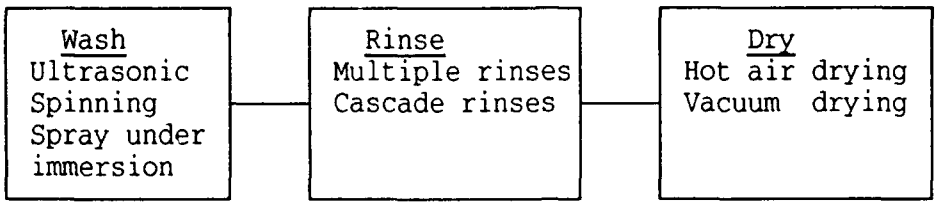
If the only requirements for an alternative cleaner were its ability to remove contamination the problem would be significantly simplified. However the effect of candidate materials on the circuit assemblies, components, operators, and its impact on the environment all must be considered. All components and formulations underwent a preliminary screening for compatibility with commonly encountered polymers, a more complete list of compatibility of formulation SL9 is given in table 3. Potential problems resulting from operator exposure to formulation SL9 has been minimised by a using materials which have no or very low toxicity classifications and which present minimal operator exposure hazard. The materials used are not readily adsorbed through the skin, minimising any health hazard through direct skin contact, and have low vapour pressures, thus offering a low inhalation hazard. Both of these risks can be further reduced by appropriately designed equipment. Risks from ingestion (either accidental or deliberate) are minimised by using low toxicity materials, as in this case.

The overall environmental impact of any material is particularly difficult to assess since there are many different possible effects. The environmental impact is reduced by using equipment designed to minimise emissions (either vapour, liquid or solid). Oxygenated solvents contain no halogen atoms and therefore have no ozone depletion potential. In the lower troposhper oxygenated solvents do undergo photochemical reactions, but their photochemical ozone generation potential (POGP) is lower than some hydrocarbons. All the materials in formulation SL9 are water miscible and will be rained out of the troposphere into the hydrosphere where they are readily biodegradable. The same fate awaits any spills which come into contact with ground water.

PROCESS OPTIONS

The ability to wash and rinse in the same medium significantly simplifies the the cleaning process. The basic process can be reduced to only 3 stages (see fig 2).

FIGURE 2 Basic Process Stages for a Single Fluid Cleaner



As can be seen from the diagram there are a number of different options within each of the three basic steps of the cleaning process

WASH

Practice has shown that the cleaning performance of formulation SL9 is improved by agitation/attrition. This can be achieved by a number of different methods. If ultrasonics are used then it is essential to have enough power to cause the fluid to cavitate .For oxygenated solvents this is 35-40 watts per litre . Spinning and spray under immersion would also provide suitable fluid agitation but have yet to be studied in detail. Practical trials have shown that effective cleaning can be achieved at temperatures of 55°C and below.

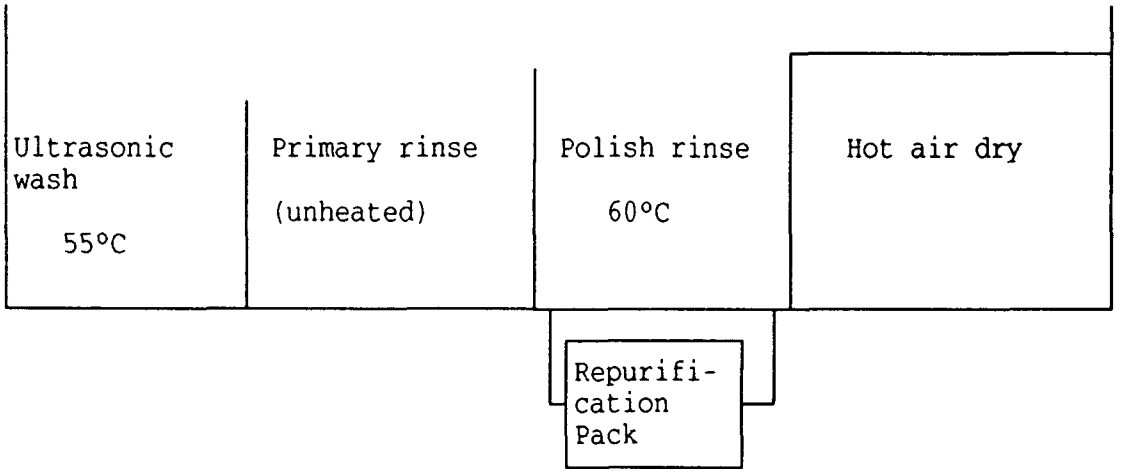
RINSE

For a number of reasons it is desirable to have multiple rinses. With only one rinse stage contamination will quickly build to a point where effective cleaning can no longer be achieved. The rate at which this occurs is highly dependent on the volume of drag-out from the wash bath, with substantial increases in bath life possible if drag-out is minimised. A simple way to reduce drag-out is to use a warm rinse, airknives can also be used if desired. A further way of prolonging the life time of the cleaner is to continuously re-purify the final rinse bath so that boards are always being rinsed in clean fluid. Re-purification of formulation SL9 can be achieved by use of appropriate ion exchange and adsorptive packs.

DRYING

In order to minimise handling and storage problems relatively non-volatile components have been used and it is therefore necessary to force dry assemblies. This can be done using conventional hot air or vacuum driers. In both cases it is necessary to work in intrinsically safe conditions. This is achieved by not exceeding the flash point of the material (in this case >100°C). Practical experiments have shown that boards can be dried under these conditions. Drying is assisted if drag-out is minimised by forced draining (e.g. air knives). A development cleaner incorporating the above ideas has been built (an outline of the process is given in fig 3)

FIGURE 3. Development Cleaner Process Equipment



All the components of formulation SL9 are both biodegradable and completely miscible with water, it could therefore be used as a semi-aqueous cleaner with water in the rinse and/or polish stages. Separation of the cleaner from the water can be achieved using adsorptive or reverse osmosis techniques where necessary.

PERFORMANCE AND PROPERTIES

The performance of formulation SL9 has been evaluated in two different processes one in the laboratory with only mild or no agitation and the other using an ultrasonics cleaner. Agitation is only necessary in the primary wash stage. The inclusion of agitation in the rinse stages does not improve performance. A typical set of cleaning data is shown in table 1 and compared with a commercial chlorinated solvent vapour degrease. The use of ultrasonics or some other suitable method for agitation of the liquid will significantly improve final board cleanliness and provide better consistency of results.(practice indicates that cleaning will improve by at least a factor of three).

TABLE 1. Preliminary Performance Data
(values are µg equivalents NaCl cm-2)

FLUX TYPES	RA	RMA	Paste	Synthetic
CLEANER				
Commercial Chorinated	4.32	3.11	1.59	0.65
FORMULATION SL9 (us)	0.75	0.65	0.16	0.08
FORMULATION SL9	3.10	2.14	0.59	0.08
FORMULATION SL9 (4 day aged flux)	1.89	1.41	0.24	-
FORMULATION SL9 (20 day aged flux)	2.96	2.01	-	-

(us) is ultrasonically assisted cleaning
Passmark is 3.1 µg equivalents NaCl cm^{-2}

NB The removal of aged flux has only been studied in the absence of ultrasonics, the results to date suggest that old flux is more difficult to remove but that it can still be cleaned to Mil Spec standards.

Preliminary surface insulation resistance (SIR) test performance data have been measured and are given in Table 2. These show that that there is no adsorption into and subsequent desorption of the cleaner from the boards, and confirms the high level of cleanliness.

Table 2. SIR Test Results

Flux	Cleaner	Surface Insulation Resistance Initial (Ω)	96 hours (Ω)
		1.70×10^{12}	1.65×10^{11}
RMA	None	1.57×10^{12}	2.17×10^{11}
	Chlorinated	3.47×10^{12}	1.93×10^{11}
	Formulation SL9	2.67×10^{12}	1.67×10^{11}
RA	None	3.07×10^{12}	2.33×10^{11}
	Chlorinated	1.83×10^{12}	2.04×10^{11}
	Formulation SL9	3.57×10^{12}	2.39×10^{11}
RA	None	3.73×10^{12}	1.43×10^{11}
	Chlorinated	4.53×10^{12}	2.00×10^{11}
	Formulation SL9	8.37×10^{12}	1.79×10^{11}

Results are average of 3 combs
Passmark (calculated) = 6.23×10^{10} Ohms

The compatibility of formulation SL9 with the common materials of construction and packaging of devices has been studied. The results are given in Table 3. The compatibility testing was carried out using both polymers and components. These were subjected to a short term warm immersion at 60°C (max. operating temperature) and a long term ambient immersion for 2 days. The effect of either of these treatments was determined both quantitatively (weight loss/gain) and qualitatively (visual inspection). Four categories of effect were created these are defined as follows:

S Suitable; 0-1% reversible weight increase and no observable solvent attack.

Sl Slight solvent attack; 1-5% reversible weight increase, observable solvent attack (e.g. crazing, softening of polymer surface).

Sw Solvent swelling; 5-10% volume increase normally reversible, no visible solvent attack.

NS Not suitable; anything worse than the above classifications.

The classification given to a particular material is the worst from either of the long or short term exposure tests. Compatibility with metals was carried out in the same way.

TABLE 3. Compatibility Data

MATERIAL	S	Sl	Sw	NS
Polyethylene (HDPE,LLDPE,LDPE)	*			
Polypropylene	*			
Polyethersulphone	*			
Polycarbonate		*		
Polystyrene		*		
Polyethyleneterephthalate	*			
Polymethylmethacrylate				*
Nylon	*			
Plastcised PVC			*	
Acrylonitrile butadiene styrene	*			
Styrene butadiene				*
Nitrile rubber, Isoprene, Natural rubber				*
Butyl, ethylene propylene rubber	*			
Fluoroelastomers	*			
Aluminium, copper	*			

CONCLUSIONS

This work has shown that matching solvent properties is an effective way of identifying potential solvent cleaners. This however in a modern society is insufficient and it is necessary to consider the health and safety aspects as well as the environmental impact of potential materials during such developments. These criteria have been

used to develop, Formulation SL9 which is simple and effective to use and represents a minimal hazard to both operators and the environment.

ACKNOWLEDGEMENTS

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RELIABILITY FIGURES OF MERIT FOR SURFACE MOUNT SOLDER ATTACHMENTS OF COMPONENTS: 2ND GENERATION GENERIC DESIGN TOOLS

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ABSTRACT

In early 1989 the original version of the Reliability Figures of Merit (FM) for the solder attachments of surface-mount (SM) assemblies was published. That version of the FMs was specifically tailored for telecommunications use environments. Misapplications of the FMs to use environments, such as military applications and accelerated tests, pointed to a real need for generally applicable FMs.

Adequate reliability of SM solder attachments can only be assured with a 'Design for Reliability' based on solder joint behavior and the underlying fatigue damage mechanisms. The perceived difficulties with a 'Design for Reliability' stem from the very complex and only partially understood nature of the interacting mechanisms underlying thermally induced solder joint fatigue combined with the highly temperature-, time-, and stress-dependent behavior of some of the involved materials, especially solder.

In this paper generic FMs are presented. These FMs are simple design tools that can easily be utilized by non-expert users unfamiliar with the underlying complexities of solder fatigue and give reliability assessment results in GO/NO-GO fashion. These FMs not only do not contain the oversimplifications -- originally thought necessary for simple design tools and limiting the applicability of the FMs -- contained in Version 1 of the FMs, but are simpler to boot.

1.0 INTRODUCTION

In early 1989 the original version (Ref. 1) of the Reliability Figures of Merit (FM) for the solder attachments of surface-mount (SM) assemblies, and shortly thereafter a somewhat improved description (Ref. 2), were published. That version of the FMs was specifically tailored for telecommunications use environments. Telecommunications use environments are characterized by cyclic frequencies of about 1 cycle/day due to day/night differences, for which enough time (dwell time ~12 hours) is available to assure essentially complete stress relaxation at both the high and low temperature dwells. The readers were explicitly admonished not to apply the FMs for use conditions that preclude

essentially complete stress relaxation within the solder joints either because of insufficient time at the cyclic temperature extremes or because of low temperatures. The readers were warned most specifically not to apply the FMs to accelerated tests since by their very nature accelerated tests do not allow enough time for complete stress relaxation.

Nevertheless, the FMs were applied to results from accelerated tests and were found to underpredict the cyclic lives; this, of course, is not a surprise, since this was stated in the caveats in Refs. 1 and 2 and is dictated by the combination of the simplifications made for the original FMs and the nature of the thermo-mechanical fatigue behavior of solder. However, the misapplications pointed to a real need for generally applicable FMs. In this paper generic FMs are presented. These 2nd generation FMs not only do not contain the oversimplifications -- originally thought necessary for simple design tools and limiting the applicability of the FMs -- contained in earlier version of the FMs, but are simpler to boot.

2.0 RELIABILITY FIGURE OF MERIT PHILOSOPHY

Adequate reliability of SM solder attachments can only be assured with an upfront 'Design for Reliability (DfR)' based on solder joint behavior and the underlying fatigue damage mechanisms. The consistency of the processing and the quality of the resulting electronic assemblies, while of course necessary, are not sufficient for reliability. Design for Reliability needs to consider the field use environment (see Table 1), the product design life, as well as the acceptable failure risk level.

The perceived difficulties with a 'Design for Reliability' stem from the very complex and only partially understood nature of the interacting mechanisms underlying thermally induced solder joint fatigue combined with the highly temperature-, time-, and stress-dependent behavior of some of the involved materials, especially solder. It is therefore necessary to formalize the procedures necessary to achieve and assure solder joint reliability into state-of-the-art, but simple to apply, tools for the 'Design for Reliability.'

The FMs provide such simple tools for 'Design for Reliability' of SM assemblies that can be used by a non-expert. These FMs can be easily utilized by users unfamiliar with the underlying complexities of solder fatigue and can give their results in GO/NO-GO fashion. While the final FM(rel) is the metrics for the assembly reliability of the component, FMs are provided at different design stages to provide additional detail if needed.

3.0 FATIGUE BEHAVIOR OF SOLDER JOINTS

3.1 EMPIRICAL RELIABILITY PREDICTION MODELS

It has been shown (Refs. 3, 4, and 5) that the fatigue life of surface mount solder joints can be described by a power law similar to the Coffin-Manson low-cycle fatigue equation (Ref. 6) developed for more typical engineering metals. For practical reasons and as the direct consequence of the time-dependent stress-

TABLE 1. Realistic Worst-Case Use Environments and Appropriate Accelerated Testing for Surface Mounted Electronics by Use Categories.

USE CATEGORY	WORST-CASE USE ENVIRONMENT						Accept.	ACCELERATED TESTING			
	Tmin °C	*Tmax* °C	ΔT (1) °C	t_D hrs	Cycles/ year	Years of Service	Failure Risk, %	*Tmin* °C	*Tmax* °C	ΔT(2) °C	t_D min
1 CONSUMER	0	+60	35	12	365	1-3	~1	+25	+100	75	15
2 COMPUTERS	+15	+60	20	2	1460	~5	~0.1	+25	+100	75	15
3 TELECOMM	-40	+85	35	12	365	7-20	~0.01	+25	+100	75	15
4 COMMERCIAL AIRCRAFT	-55	+95	20	12	365	~20	~0.001	0	+100	100	15
5 INDUSTRIAL& AUTOMOTIVE -PASSENGER COMPARTMENT	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	~10	~0.1	0	+100	100	15
								& "COLD(3)"			
6 MILITARY GROUND&SHIP	-55	+95	40 &60	12 12	100 265	~5	~0.1	0	+100	100	15
								& "COLD(3)"			
7 SPACE leo	-40	+85	35	1	8760	5-20	~0.001	0	+100	100	15
7 SPACE geo				12	365						
								& "COLD(3)"			
8 MILITARY AVIONICS a	-55	+95	40	2	365	~10	~0.01	0	+100	100	15
8 MILITARY AVIONICS b			60	2	365						
8 MILITARY AVIONICS c			80	2	365						
			&20	1	365			& "COLD(3)"			
9 AUTOMOTIVE -UNDER HOOD	-55	+125	60	1	1000	~5	~0.1	0	+100	100	15
			&100	1	300						
			&140	2	40			& "COLD(3)" & "LARGE ΔT(4)"			

& = in addition

(1) ΔT represents the maximum temperature swing, but does not include power dissipation effects; for power dissipation calculate ΔT_e; power dissipation can make pure temperature cycling accelerated testing significantly inaccurate.

(2) All accelerated test cycles shall have temperature ramps <20°C/min and dwell times at temperature extremes shall be 15 minutes measured on the test boards. This will give ~24 cycles/day.

(3) The failure/damage mechanism for solder changes at lower temperatures; for assemblies seeing significant cold environment operations; additional "COLD" cycling from perhaps -40 to 0°C with dwell times long enough for temperature equilibration and for a number of cycles equal to the "COLD" operational cycles in actual use is recommended.

(4) The failure/damage mechanism for solder is different for large cyclic temperature swings traversing the stress-to-strain -20 to +20°C transition region; for assemblies seeing such cycles in operation, additional appropriate "LARGE ΔT" testing with cycles similar in nature and number to actual use is recommended.

relaxation/creep behavior of the solder at typical use environments (see Table 1), the specialized case of the Coffin-Manson equation requires reversion to the more general relationship of Morrow (Ref. 7); it also requires that the cyclic strain energy be based on the total possible thermal expansion mismatch and that the exponent is a function of temperature and time to provide a measure of the completeness of the stress-relaxation process.

The fatigue life, $N_f(x\%)$ of surface mount solder attachments at a given acceptable failure probability, x, and thus the reliability, of surface mount (SM) solder attachments can be predicted for both isothermal-mechanical and thermal cycling (Ref. 8). These predictions are for typical realistic use conditions and representative accelerated tests, and are subject to the caveats listed later in this section. For stiff leadless SM solder attachments, for which the stresses in the solder joints exceed the solder yield strength, the predictive equation is

$$N_f(x\%) = \frac{1}{2}\left[\frac{2\varepsilon_f'}{F}\frac{h}{L_D\,\Delta\alpha\,\Delta T_e}\right]^{-\frac{1}{c}}\left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{\frac{1}{\beta}} \tag{1}$$

For compliant leaded solder attachments, where the solder joint stresses are below the yield strength and thus are not bounded by it, the predictive equation is

$$N_f(x\%) = \frac{1}{2}\left[\frac{2\varepsilon_f'}{F}\frac{(200\text{ psi})Ah}{K_D\,(L_D\,\Delta\alpha\,\Delta T_e)^2}\right]^{-\frac{1}{c}}\left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{\frac{1}{\beta}} \tag{2}$$

where for metric units the scaling *coefficient* is 1.38 MPa instead of 200 psi, where for near-eutectic tin/lead (63/37 and 60/40) solders (for other solders the coefficients are expected to have different values)

$$c = -0.442 - 6\text{x}10^{-4}\overline{T_{SJ}} + 1.74\text{x}10^{-2}\ln\left(1+\frac{360}{t_D}\right) \tag{3}$$

and where

- A = effective minimum load bearing solder joint area ($\equiv$2/3 solder-wetted lead area projecting to solder pad),
- c = fatigue ductility exponent defined in Eq. 3,
- F = empirical "non-ideal" factor indicative of deviations of real solder joints from idealizing assumptions and accounting for secondary and frequently intractable effects such as cyclic warpage, cyclic transients, non-ideal solder joint geometry, brittle intermetallic compounds, Pb-rich boundary layers, and solder/bonded-material expansion differences, as well as inaccuracies and uncertainties in the parameters in Eqs. 1 and 2; $1.5>F>1.0$ for column-like leadless solder attachments, $1.2>F>0.7$ for leadless solder attachments with fillets (castellated chip carriers and chip components), $F\approx 1$ for solder attachments utilizing compliant leads;
- h = solder joint height, for leaded attachments $h\equiv 1/2$ of solder paste stencil depth as a representative dimension for the average solder thickness,

K_D = "diagonal" flexural stiffness of unconstrained, not soldered, component lead, determined by strain energy methods (see Refs. 9, 10, 11 and 12) or finite element analysis,

$2L_D$ = maximum distance between component solder joints measured from component solder joint pad centers,

N = (design life times cyclic frequency), number of operating cycles during product life,

$N_f(x\%)$ = number of operating cycles to $x\%$ failure probability,

T_C, T_S = steady-state operating temperature for component, substrate ($T_C > T_S$ for power dissipation in component) during high temperature dwell,

$T_{C,0}, T_{S,0}$ = steady-state operating temperature for component, substrate during low temperature dwell, for non-operational (power off) half-cycles $T_{C,0} = T_{S,0}$,

$\overline{T_{SJ}}$ = $(1/4)(T_C+T_S+T_{C,0}+T_{S,0})$, mean cyclic solder joint temperature,

t_D = half-cycle dwell time in minutes, average time available for stress relaxation at T_C/T_S and $T_{C,0}/T_{S,0}$,

x = acceptable cumulative failure probability for the component under consideration after N cycles, %,

α_C, α_S = coefficient of thermal expansion (CTE) for component, substrate,

β = Weibull shape parameter, slope of Weibull probability plot, typically 4 for stiff leadless attachments and 2 for compliant leaded attachments,

ΔT_C = $T_C - T_{C,0}$, cyclic temperature swing for component,

ΔT_e = $[(\alpha_S \Delta T_S - \alpha_C \Delta T_C)/\Delta\alpha]$, equivalent cycling temperature swing, accounting for component power dissipation effects as well as component external temperature variations ($\Delta\alpha \neq 0$),

ΔT_S = $T_S - T_{S,0}$, cycling temperature swing for substrate (at component),

$\Delta\alpha$ = $|\alpha_C - \alpha_S|$, absolute difference in coefficients of thermal expansion of component and substrate, CTE-mismatch,

ε_f' = fatigue ductility coefficient, $2\varepsilon_f' \approx 0.65$ for eutectic and 60/40 Sn/Pb solder (for other solders the value of ε_f' is expected to be different).

Equations 1 and 2 contain all the first-order parameters influencing the shear fatigue life of solder joints and come from a generic understanding of the response of surface mount solder joints to cyclically accumulating fatigue damage resulting from shear displacements due to thermal expansion mismatches between component and substrate. These shear displacements -- the global thermal expansion mismatch -- cause time-independent yielding strains and time-, temperature-, and stress-dependent creep/stress relaxation strains (Refs. 8 and 13). These strains, on a cyclic basis, form a visco-plastic strain energy hysteresis loop which characterizes the solder joint response to thermal cycling and whose area is indicative of the cyclically accumulating fatigue damage. Hysteresis loops in the shear stress-strain plane have been experimentally obtained (Refs. 5, 14, 15, and 16). In Eqs. 1 and 2 A, h, K_D, and L_D are physical design parameters, $\Delta\alpha$ depends on the material properties of component and substrate, ΔT_e reflects the component-external environmental and thermal conditions as well as the component-internal power dissipation, c in Eq. 3 accounts for the degree of completeness of the cyclically recurring stress

relaxation process in the solder joints (the coefficients in c as well as ε_f' are dependent on the solder composition -- the values given are for 60 Sn/40 Pb and eutectic Sn/Pb solder), and β is the slope of the Weibull statistical failure distribution.

3.2 FAILURE DEFINITION

In this context, failure is defined as the interruption of electrical continuity ($\geq$300 Ω) even for only very short durations ($\geq$1 μsec) (Ref. 17). The "non-ideal" factor, F, is the only parameter reflecting specific design- and processing-induced influences on fatigue reliability and needs to be determined empirically from the difference in the prediction of fatigue life from Eqs. 1 or 2 for idealized solder attachments ($F=1$), and the fatigue life obtained empirically from accelerated testing. It should be noted that it is not altogether clear whether the F-values obtained from accelerated tests are necessarily the same for cyclic use environments, which typically allow more complete cyclic stress relaxation.

3.3 MULTIPLE CYCLIC LOAD HISTORIES

Multiple cyclic load histories (e.g. "Cold" temperature fatigue cycles combined with higher temperature creep/fatigue cycles (see Table 1) combined with vibration) all make their contributions to the cumulative fatigue damage in solder joints. Under the assumption that these damage contributions are linearly cumulative -- this assumption underlies Eqs. 1 and 2 as well -- and that the simultaneous occurrence or the sequencing order of these load histories makes no significant difference, the Palmgren-Miner's rule (Ref. 18) can be applied,

$$\sum_{1}^{i} \frac{N_i}{N_{f,i}} \leq 1 \tag{4}$$

where

N_i = actually applied number of cycles at a specific cyclic load level i,

$N_{f,i}$ = fatigue life at the acceptable failure probability from the same specific cyclic load level i alone.

Equation 4 can be used with the allowable sum of the fatigue damage fractions significantly less than unity to provide margins of safety.

3.4 CAVEAT 1 - SOLDER JOINT QUALITY

The solder joint fatigue behavior and the resulting reliability prediction relationships, Equations 1 and 2, were determined from thermal cycling results of solder joints that failed as a result of fracture of the solder, albeit sometimes close to the intermetallic compound (IMC) layers. For solder joints for which layered structures are interposed between the base material and the solder joints, these equations could be optimistic upper bounds if the interposed layered structures become the "weakest link" in the surface mount attachments. Such layered structures could be: metallization layers that have weak bonds to the underlying material, or are weak themselves, or dissolve essentially completely in the solder; oxide or contamination layers preventing proper metallurgical

bond of the solder to the underlying metal; brittle intermetallic compound layers too thick due to elevated temperature processing steps, perhaps because of too long durations, too high temperatures, and/or too many such steps.

3.5 CAVEAT 2 - LARGE TEMPERATURE EXCURSIONS

It should be noted that solder joints seeing large temperature swings significantly below and above the temperature region from -20 to +20°C in which the change from stress-to-strain driven solder response takes place, do not follow the the damage mechanism described in Eqs. 1 and 2 (Ref. 19). The damage mechanism is different than for more typical use conditions and is likely dependent on overstress and recrystallisation considerations.

3.6 CAVEAT 3 - HIGH FREQUENCY/LOW TEMPERATURES

For high-frequency applications, $f > 0.5$ Hz or $t_D < 1$ sec, and/or low temperature applications, $T_C < 0°C$, for which the stress relaxation and creep in the solder joint is not the dominant mechanism, the direct application of the Coffin-Manson fatigue relationship (Ref. 6) is advised. This relationship, modified to include the statistical failure distribution, is

$$N_f(x\%) = \frac{1}{2}\left[\frac{\Delta\gamma_p}{2\varepsilon_f'}\right]^{\frac{1}{c}}\left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{\frac{1}{\beta}} \tag{5}$$

where $\Delta\gamma_p$ = cyclic plastic strain range,
c = ≈-0.6,
β = ≈3.

3.7 CAVEAT 4 - LOCAL EXPANSION MISMATCH

For applications for which the global thermal expansion mismatch is very small, e.g. ceramic-on-ceramic or silicon-on-silicon (flip-chip solder joints), the local thermal expansion mismatch becomes the primary cause of fatigue damage. Equations 1 and 2 do not address the local thermal expansion mismatch. This reliability problem needs to be assessed using an interfacial stress analysis (Ref. 20) and appropriate accelerated testing.

3.8 CAVEAT 5 - LEAD CTE MISMATCH

It should be noted, that for leaded components with lead materials that have CTEs significantly lower than copper alloy materials, e.g. Kovar, Alloy 42, the results from Eq. 2 will be optimistic, since the fatigue damage contributions from the solder/lead material CTE-mismatch, the local thermal expansion mismatch, are not included.

4.0 RELIABILITY FIGURES OF MERIT

Designing electronic products requires many trade-offs among frequently conflicting requirements. The designer needs to consider, among others,

functionality, availability, manufacturability, testability, yield, cost, weight (in the case of airborne equipment), and reliability. Thus , simple tools for the designer, who cannot be an expert in all these areas, are essential.

Reliability Figures of Merit - **FM**s are simple relative measures of the reliability potential of the SM solder attachment of a component or assembly design. They provide designers with a guide for the selection of components and the design of assemblies for particular applications and the use conditions for these applications. The **FM**s provide the basic design tools for a "Design for Reliability" of product using surface mount technology. Figure 1 shows in a flow chart SM solder attachment reliability assurance where the "Design for Reliability" fits into the reliability assurance process for a specific product. The reliability **FM**s provide the link between the generic understanding of solder joint fatigue behavior gained from controlled experiments and analytical insights and the need to convert this knowledge to practical realization for solder attachment reliability. It need to be emphasized that these simple design tool **FM**s cannot replace a comprehensive "Design for Reliability" procedure, which has to include the effects of the attachments of all the components in the system as well as perhaps the effects of multiple environments and loading conditions.

FMs need to be easily determined and interpreted by users unfamiliar with the details and complexities of SM solder attachment reliability. **FM**s would serve their intended purpose best by : 1) being dimensionless to facilitate easy comparisons, 2) being numerically near to or greater than unity for reliable designs to provide an easy design target, and 3) signify higher reliability by increasing numerical values to provide the psychologically correct directionality. Further, the **FM**s at the different design stages should lead to one another from design-stage to design-stage to provide easy and logical design continuity.

The relative assessment of the reliability potential is needed during two stages in the design sequence: component selection, and substrate selection, which determines the global expansion mismatch potential for the assembly. Adding the application-specific thermal use conditions determines the actual global thermal expansion mismatch, and the reliability of the design can be evaluated with the addition of the the reliability requirements for the product. Consequently, **FM**s were developed for these different design stages:

- **FM**(comp) - for the reliability impact of the *component* selection,
- **FM**(assy) - for the reliability impact of the component/substrate *assembly* design,
- **FM**(env) - for the reliability impact of the application-specific thermal use *environment* conditions,
- **FM**(rel) - for the *reliability* impact of the application-specific product life, use conditions, and acceptable failure risk.

Together with other important physical parameters, like component dimensions, coefficient of thermal expansion (CTE), and lead stiffness, **FM**(comp)

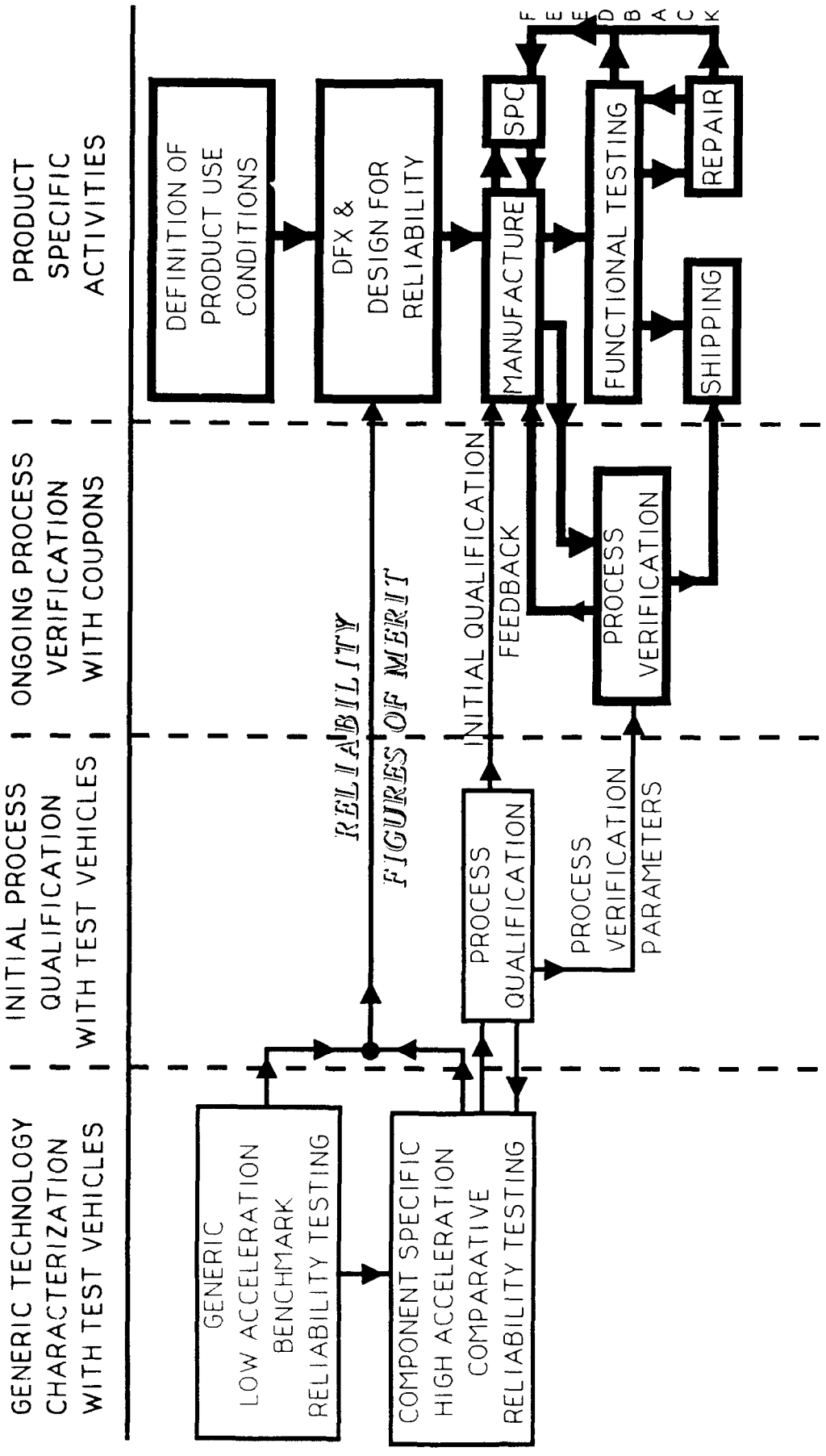

Figure 1 - Flow chart for surface mount solder attachment reliability assurance showing the need for reliability design information provided by the Reliability Figures of Merit "Design for Reliability" tools.

should become part of the data sheet information for each component. Currently, these parameters need to be determined by measurement and calculation by the users of the components.

4.1 FM(comp)s FOR COMPONENT SELECTION

The component parameters that impact SM solder attachment reliability are:

- choice of attachment type -- leadless or leaded
- if leadless, the metallization design and the resulting solder joint height:
  - ➡ single-surface pad (e.g. non-castellated chip carriers, flip-chip joints, pad arrays) allow swimming up of component for solder joint heights of ~10 mils
  - ➡ multi-surface metallisations (e.g. castellated chip carriers, discrete chip components) preventing swimming up of component resulting in solder joint heights of ~3 mils
- if leaded, the lead stiffness (see Refs. 9 through 12), the minimum load bearing solder joint area, and the solder paste stencil thickness (solder volume)
- component size
- component material(s), and thus the effective coefficient of thermal expansion.

From the above considerations, the **FM**s for the component selection are formulated as

$$\mathbf{FM}(\text{comp, ll}) \equiv 20\frac{h}{L_D}, \qquad \text{for leadless attachments} \quad (6)$$

and

$$\mathbf{FM}(\text{comp, ld}) \equiv (1\text{x}10^7\text{psi})\frac{Ah}{K_D L_D^2} \qquad \text{for leaded attachments.} \quad (7)$$

It should be noted, that the coefficient values in Eqs. 6 and 7, as well as in Eqs. 8 through 11 in the subsequent sections, do not have a physical significance other than scaling the intermediary **FM**s towards unity.

4.2 FM(assy)s FOR SUBSTRATE SELECTION

The thermal expansion coefficient of the substrate, together with the CTE of the component, determines the difference in coefficients of thermal expansion between component and substrate, $\Delta\alpha$. Thus, each different component in the assembly will have its own **FM**(assy), given by

$$\mathbf{FM}(\text{assy, ll}) \equiv \mathbf{FM}(\text{comp, ll}) \frac{(4\ \text{ppm/°C})}{\Delta\alpha}, \quad \text{for leadless attachments} \quad (8)$$

and

$$\mathbf{FM}(\text{assy, ld}) \equiv \mathbf{FM}(\text{comp, ld}) \left[\frac{(5\ \text{ppm/°C})}{\Delta\alpha}\right]^2, \text{ for leaded attachments.} \quad (9)$$

4.3 FM(env)s FOR THERMAL USE CONDITIONS

The reliability of a SM solder attachment will primarily be determined by the **FM**(assy), together with the thermal use conditions. The thermal use conditions may have to be determined using a thermal analysis of the whole system and will primarily depend on the power dissipation within the component analyzed, the thermal conditions within the system external to the component analyzed, and the the thermal environment external to the system. The combined impact of the power dissipation and the operating environment is captured in the cyclic differential thermal expansion between component and substrate, $\Delta\alpha\Delta T_e$. Since the CTE-mismatch $\Delta\alpha$ is part of **FM**(assy), the environment-level **FM** is formulated as

$$\mathbf{FM}(\text{env, ll}) \equiv \mathbf{FM}(\text{assy, ll}) \frac{(40°\text{C})}{\Delta T_e}, \quad \text{for leadless attachments} \quad (10)$$

and

$$\mathbf{FM}(\text{env, ld}) \equiv \mathbf{FM}(\text{assy, ld}) \left[\frac{(50°\text{C})}{\Delta T_e}\right]^2, \quad \text{for leaded attachments.} \quad (11)$$

4.4 FM(rel)s FOR ASSEMBLY RELIABILITY ASSESSMENT

The interim **FM**s deal with the design and the loading conditions for the solder attachment assembly. The **FM**(rel)s include some loading condition parameters in the form of the mean cyclic temperature and the cyclic dwell time. These two parameters determine the degree of completeness of the stress relaxation process, which converts elastically stored strain energy into plastic deformations in the solder joints; they determine the value of the exponent, c. Whether or not a design is reliable for its intended product use depends on the product design life, and the allowable failure risk at the end of the design life. The product life and the cyclic frequency result in an expected product cyclic life of N cycles of operation. The **FM**(rel) formulations are then

$$\mathbf{FM}(\text{rel, ll}) \equiv \mathbf{FM}(\text{env, ll}) \frac{1}{(2N)^{-c}} \frac{2\varepsilon_f'}{3200F} \left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{-\frac{c}{\beta}}, \quad (12)$$

for leadless attachments and for leaded attachments

$$\mathbf{FM}(\text{rel, ld}) \equiv \mathbf{FM}(\text{env, ld}) \frac{1}{(2N)^{-c}} \frac{2\varepsilon_f'}{3.125\text{x}10^9 F} \left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{-\frac{c}{\beta}}. \quad (13)$$

In many cases, it will be advantageous to calculate **FM**(rel) directly. The formulations without the intermediary **FM**s are

$$\mathbf{FM}(\text{rel, ll}) \equiv \frac{1}{(2N)^{-c}} \frac{2\varepsilon_f'}{F} \frac{h}{L_D \Delta\alpha \Delta T_e} \left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{-\frac{c}{\beta}}, \quad (14)$$

for leadless attachments and for leaded attachments

$$\mathbf{FM}(\text{rel, ld}) \equiv \frac{1}{(2N)^{-c}} \frac{2\varepsilon_f'}{F} \frac{(200\text{psi})Ah}{K_D (L_D \Delta\alpha \Delta T_e)^2} \left[\frac{\ln(1-0.01x)}{\ln(0.5)}\right]^{-\frac{c}{\beta}}. \quad (15)$$

If Eqs. 1, 2, 14, and 15 are examined, it is evident that the **FM**(rel)s are simply the ratio of the number of operating cycles to the acceptable cumulative failure probability $x\%$ and the number of product life cycles, to the power of $-c$,

$$\mathbf{FM}(\text{rel}) \equiv \left[\frac{N_f(x\%)}{N}\right]^{-c} \quad (16$$

It should be noted, that the **FM**(rel)-equations deal explicitly only with the effects of the global thermal expansion mismatch between components and substrates; for leads made of metals other than copper alloys having coefficients of thermal expansion significantly below 18 ppm/°C, lower SM solder attachment reliability than predicted by Eqs. 13 and 15 has to be expected due the local thermal expansion mismatch between the lead material and the solder.

4.5 DESIGN RELIABILITY ASSESSMENT USING FM(rel)s

The **FM**(rel)-equations have been formulated to the following reliability criteria:

FM(rel) ≥ 1.0..... reliability requirements are met with this design

FM(rel) ≤ 0.7..... current design cannot meet reliability requirements; design changes are required

0.7 < **FM**(rel) < 1.0..... design might become reliable with relative small reductions in the reliability requirements or more accurate determination of some of the other parameters.

The application of the reliability **FM**s can be illustrated using the flow chart in Figure 2. Figure 2 shows that the use of **FM**(comp), **FM**(assy), and **FM**(env) is

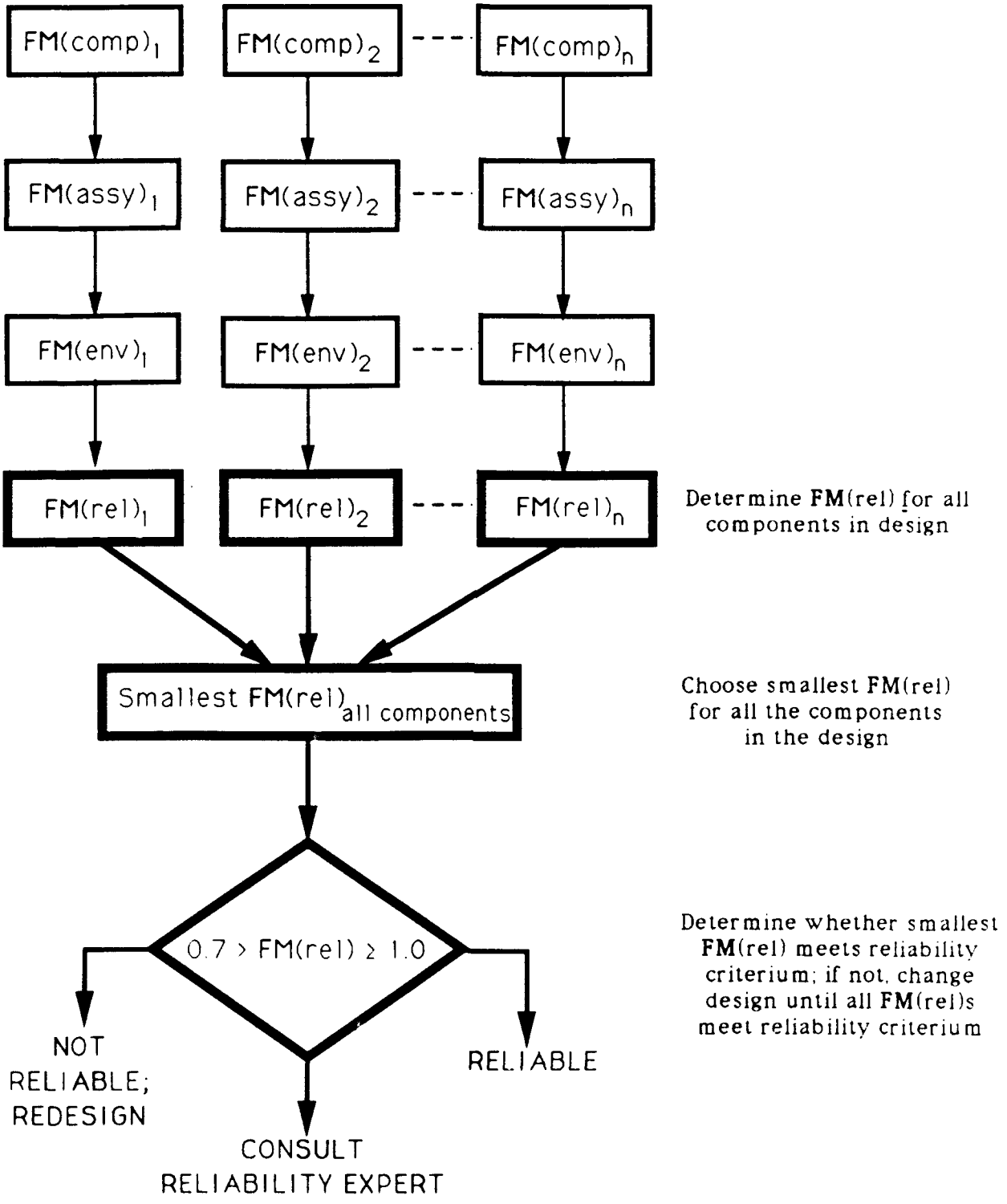

Figure 2 - Application flow chart for surface mount solder attachment reliability Figures of Merit.

not essential; however, FM(rel) needs to be determined and the design changed until the FM(rel)s for all components meet the reliability criterion.

5.0 RELIABILITY FIGURES OF MERIT DERATING SYSTEM

In part of the industry derating systems have been found useful. The reliability FMs can be utilized to for these purpose with the definition of a set of reference conditions. Equations 17 to 20 give FM(rel) derating functions for situations where one parameter is to be altered.

Equation 17 is for the case where the product design life needs to be changed,

$$\frac{\mathbf{FM(rel)}}{\mathbf{FM(rel)}|_{Ref}} \propto \left[\frac{N}{N|_{Ref}}\right]^{c} \tag{17}$$

Assuming a doubling of the design life without a change in the cycle frequency and shape, FM(rel) would be derated to 71% in the case of slow, high temperature use cycles (1 cycle/day @ $\overline{T_{SJ}}$ = 85°C), and to 75% in the case of fast, low temperature use cycles (12 cycles/day @ $\overline{T_{SJ}}$ = 15°C).

Equation 18 is for the case where the thermal use conditions need to be changed,

$$\frac{\mathbf{FM(rel)}}{\mathbf{FM(rel)}|_{Ref}} \propto \left.\frac{\Delta T_e|_{Ref}}{\Delta T_e}\right|_{leadless}; \propto \left.\left[\frac{\Delta T_e|_{Ref}}{\Delta T_e}\right]^{2}\right|_{leaded} \tag{18}$$

Here different relationships are required for leadless and leaded SM solder attachments; a doubling of the ΔT_e results in a derating of FM(rel) to 50% in the case of leadless SM attachments and to 25% for leaded SM attachments.

Equation 19 is for the case where the acceptable cumulative failure probability at the end of the design life needs to be changed,

$$\frac{\mathbf{FM(rel)}}{\mathbf{FM(rel)}|_{Ref}} \propto \left[\frac{\ln(1-0.01x)}{\ln(1-0.01x|_{Ref})}\right]^{\frac{c}{\beta}} \tag{19}$$

An decrease in the acceptable cumulative failure probability by a factor of ten (10) leads to the following FM(rel) deratings:

Leadless: to 76% for slow, high temperature use cycles (1 cycle/day @ $\overline{T_{SJ}}$ = 85°C),
to 79% for fast, low temperature use cycles (12 cycles/day @ $\overline{T_{SJ}}$ = 15°C),
Leaded: to 57% for slow, high temperature use cycles (1 cycle/day @ $\overline{T_{SJ}}$ = 85°C),
to 62% for fast, low temperature use cycles (12 cycles/day @ $\overline{T_{SJ}}$ = 15°C).

Equation 20 is for the case where a change in mean cyclic temperature or/and in the cyclic dwell time is needed.

$$\frac{\mathbf{FM(rel)}}{\mathbf{FM(rel)}|_{Ref}} \propto [2N]^{c-c|_{Ref}} \left[\frac{\ln(0.5)}{\ln(1-0.01x)}\right]^{\frac{c-c|_{Ref}}{\beta}} \tag{20}$$

Assuming a product cyclic life of 3650 cycles and an acceptable cumulative failure probability at the end of the design life of 0.01%, **FM**(rel) would be derated to 47% and 40% for leadless and leaded SM attachments, respectively, for a change from fast, low temperature use cycling (12 cycles/day @ $\overline{T_{SJ}}$ = 15°C) to slow, high temperature use cycles (1 cycle/day @ $\overline{T_{SJ}}$ = 85°C).

6.0 SUMMARY

Reliability Figures of Merit (**FM**s) have been developed to provide simple to use design tools for the necessary upfront "Design for Reliability" to assure the long-term reliability of Surface Mount (SM) solder attachments. These **FM**s are in a form that does not require expertise in solder fatigue nor judgmental evaluation for their utilization. The answers are in GO/NO-GO form.

- **FM**s have been developed to provide "Design for Reliability" tools at critical stages in the SM product development.
- **FM**s combine design parameters and product life data in the form of simple design tools.
- **FM**s allow the assessment of the interplay and the effects of the various parameters influencing the SM solder attachment reliability.
- **FM**s show that SM solder attachments can be designed to be reliable. For severe use conditions, long product lives, and low acceptable failure probabilities, the design options may be limited.
- **FM**s assure the long-term reliability at the design stage; low-quality SM solder attachments due to substitutions in component or printed circuit board materials, solderability problems, inadequate soldering processes, or abuse product testing or repair will reduce the reliability of the product.

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SOLDERING, REWORKING AND INSPECTING A TWENTY-TWO LAYER MASTER INTERCONNECT BOARD.

by

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ABSTRACT

The objective of the development effort was to establish a wave solder, a rework and an inspection process for a 22 layer master interconnect board (MIB) used on the Space Shuttle Main Engine Controller (SSMEC) Program. The MIB is atypical in size with 11,766 solder joints. Initially the board was wave soldered with a process yield of less than 50%.

In the development of a better wave solder process several problems were encountered with equipment, material and board plating that had to be overcome. The size of the board was the first hurdle that presented itself in terms of ensuring that existing equipment could accommodate the MIB. Following resolution of equipment problems, much emphasis was placed on working with the MIB vendors in resolving material and plating problems which were inhibiting improvements to the process.

Reworking unacceptable plated-through-holes is accomplished utilizing a custom hot plate designed and fabricated exclusively for the MIB. Visual inspection of the top side solder joints is virtually impossible due to the connector/pin configuration. Inspection is accomplished utilizing microfocus radiography.

The efforts have been outstanding in that the MIB soldering process yield is now at 99+ %, the cycle time has been reduced from twelve to six weeks and board quality is outstanding.

INTRODUCTION

Understanding the problems in the development of various processes on a twenty-two layer board begins with the board parameters generated during the initial design. Parameters were successively changed as the board evolved to its present configuration.

There were 3 major steps in the evolution of the MIB's material. The original board design and manufacture was of a GF difunctional glass laminate which gained and lost heat relatively quickly making the wave solder process a repeated "stop and go" routine, at best, for this size board.

A design change brought a second material to the MIB which was a GF composite also, and was chosen for what was thought to be sufficiently improved z axis expansion characteristics. Unique cross lining in the polymers made this tetrafunctional glass epoxy a more thermally stable material from which the MIB could be wave soldered. This was an advantage that was never realized probably due to the sheer mass of the MIB and some of the large copper planes/heat sinks within the MIB. Equally important to the thermal advantage provided by the tetrafunctional material was the fact that both the difunctional and tetrafunctional materials were classified "GF" in the MIL-P-13949 specifications. This would allow a change of materials without resubmitting the board to qualification testing. Gaining an improved material without having to requalify was a reasonable path to pursue.

Following the change in material, three of the original difunctional flight MIB's remained in the supply line that had to be processed and appropriate parameters were worked out to wave solder these boards. The tetrafunctional material was only slightly more forgiving in its capacity to gain and lose temperature and consequently was only somewhat less difficult to process than the difunctional material. Neither material was anywhere close to an ideal process for the size pwb that was being worked. Fortunately there was only one flight level tetrafunctional MIB in the supply loop and eventually the MIB was laminated with a GI polyimide glass material. Portions of the wave solder process developed for GF boards were common to many materials and these were carried over to the polyimide wave solder process. Although the GI polyimide required a resubmit for qualification testing, the advantages gained in processability far outweighed any problems with requalifying the MIB with polyimide. Polyimide was chosen almost exclusively for its durable characteristics and in this application it performed very well on this board. Specifically, the z-axis expansion characteristics allow it to endure the high stress environment both in the wave solder and rework operations.

The third material change, and certainly the most significant, was reducing the laminate thickness from 10 mil polyimide to 8 mil polyimide. With the reduced laminate the board thickness range dropped from 0.230 - 0.270 inches to a range of 0.180 - 0.210 inches with 80% of the boards that were wave soldered after the change being 0.190 ± 0.005 inches. The laminations change, in turn, altered the aspect ratio from 6:1 to 4:1. The change in board thickness made the MIB relatively easier to manage through the soldering operations, but also required the revision of most every step in the various processes that specified a temperature.

Common to all the material changes was the marginal availability of tooling boards with which to develop any of the processes. Although lack of tooling is probably the bane of many development projects, the MIB incurred the additional problem of plating anomalies with each material change, first with one vendor and then with the other. Determining whether these solder problems were board related or process related became a "best guess" situation until sufficient tests could be run on boards and process parameters could be checked. "Flexible" was a key word in this development. Many of the plating problems were alleviated with the 8 mil laminated boards. Boards produced through the remainder of the program and any spare contracts will be filled with the 8 mil polyimide boards.

The processes, which have been evolving continuously from the start, now produce very high quality boards requiring a minimum of rework and complete the MIB assembly in less than half the time necessary to finish the product 3 years ago. And while the processes being used are not unique either to the board manufacture or the board processing, what did change was how to apply 10 layer technology to a 22 layer MIB.

THE BOARD

The Master Interconnect Board (MIB) is a printed wiring board 1.8 feet long, 1.1 feet wide and 0.190 inches thick. There are 11,766 solder joints: 10,546 of the solder joints are wave soldered and 1,220 are hand soldered (ref. Table 1). Solder joints are filled from both sides of the board with the 1,096 solder joints of the "J" connectors shown in Table 1 hand soldered from the layer 22 side of the board. The majority of the remaining solder joints are wave soldered from the layer 1 side.

A schematic drawing of the standard plated-through-hole configuration used on the MIB is shown in Figure 1. The configuration consists of a 0.045 inch drilled PTH with an aspect ratio presently of 4:1 diameter of drilled hole to board thickness. The holes are copper plated 1.5 mils minimum to the center of the hole with pads at 0.070 inches diameter.

Traces on the signal layers are etched from a mixture of 1.4 mil thick (1 oz/ft^2) and 2.8 mil thick (2oz/ft^2) copper clad GI polyimide glass laminations which are 8 mils thick. The high current capacity traces on the power and ground plane layers are from the 2.8 mil thick (2 oz/ft^2) copper. The copper clad in the hole is a standard 2 stage process with an initial electroless copper strike followed by an electroplate of copper for overall thickness. The barrels and traces are then tin/lead plated to provide the etch resist (0.3 mils minimum), so desired features are not etched away.

Table 1. PTH's on MIB Requiring Solder

Use of Plated-Through-Hole	Wave Soldered	Hand Soldered	Totals
"A" body (daughter board) connector holes	9,936		9,936
via's	610		610
"J" body (signal line) edge connector holes		1,096*	1,096
Input Cables		124	124
Totals	10,546	1220	11,766

*Soldered from layer 22 side

Initially board weight was used as a process indicator as to the amount of heat that would be required to wave solder the MIB to an acceptable level. The greater the board mass the higher the temperatures would be set throughout the process. The temperature requirements in the rework operations were also adjusted higher based on a board's mass. Currently the weight is used as a flag to uncover any problems that have gone undetected. Problem detection through weight comparison is a leftover fail-safe from a more paranoid period.

Board weight throughout the process is as noted in Table 2 below.

Table 2. Board Weight Through Processing

Process Step	kg	lb
As Received	1.9	4.2
Loaded with Connectors prior to Wave.	3.8	8.4
With all Connectors soldered	4.0	8.8
As stocked	4.7	10.3

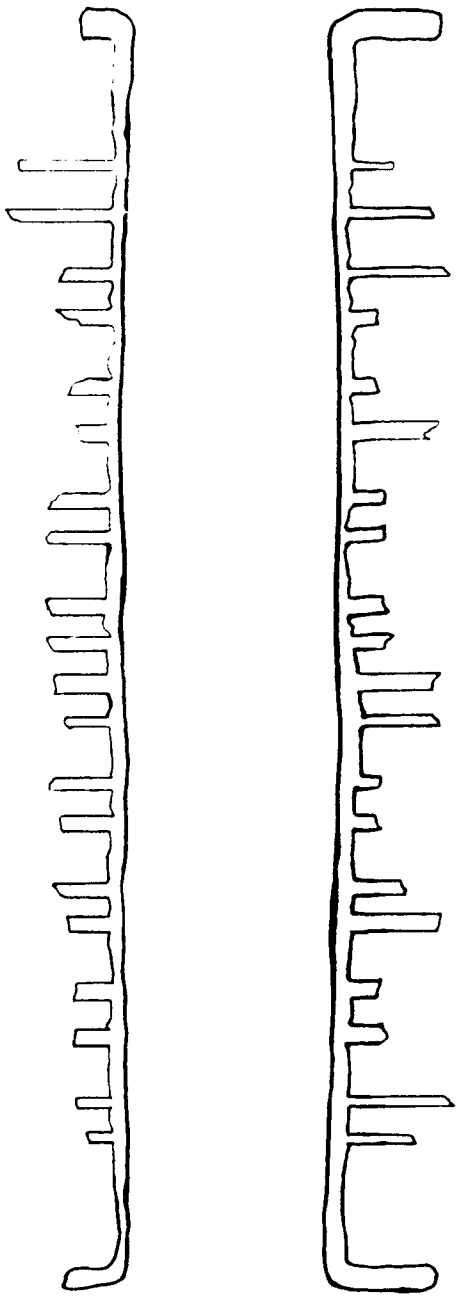

FIGURE 1
CROSSECTION OF
MIB PLATED
THROUGH HOLE

THE PROCESSES

The development of the various MIB processes took on a priority that is listed below. Occasionally the list of priorities would be redirected, but they never remained redirected for any length of time. The development team needed to be able to:

1) achieve acceptable fill in pth's using wave solder;

2) accurately check for pth fill;

3) clean and dry the boards thoroughly and consistently;

4) have a rework method for pth's with insufficient fill;

5) reduce the visual/surface defects resulting from wave solder.

There were 4 major problems encountered with developing the processes for the MIB:

1) the board itself as supplied by vendors with its multiple base materials, thickness variation and plating problems;

2) the development of the wave process including finding an available and adequate machine, then establishing wave parameters with the limited number of tooling boards and redefining parameters with each board revision;

3) insuring after wave that, in fact, the wave solder process had produced good joints even though visibility on the component side of the board was limited to less than 25%; and

4) developing a rework process that would not damage the board or the good joints produced on the wave.

VENDOR PROCESS DEVELOPMENT

Some of the problems involving the design changes and the vendor problems were reviewed in the introduction. Partial source of many of the headaches was a lack of experience in designing, building and processing a board as large as the MIB. Vendor problems fell into 3 categories; registration, drilling and plating. All three categories were plagued with inconsistency. Registration would be good in one process step but not in another and when registration was good on a number of boards those might be lost in the drilling or plating operations. Then, when the drilling was correct, boards were lost to registration and plating, each operation in its turn reducing the output to very limited numbers. There undoubtedly were countless other problems, but these three operations most influenced the minimum supply of MIB's. Common to all 3 categories was the problem of the MIB's physical size. Problems in registration due to board size might be obvious, but board size also affected plating ratio distribution and drilling set up.

While registration of 22 layers is about 20% harder than a more normal 10 layer board, accomplishing registration when the inch per inch stability factors of the material and film on a board the size of the MIB are factored in, the registration becomes twice as hard to accomplish and still maintain the desired quality. Following the etching operation for example, inner layers grow 18 mils and shrink back some 12 mils after bakeout only to resume the original dimension following the bake. Both layer to layer and hole to pad registration are significantly affected by the size of the board.

Considerable effort went into determining the optimum feeds and speeds for the hole drilling operation. Drill bit supplies were changed, drill bit design was modified and one of the most important process alterations was in the drill setup. The MIB is bolted to the drill table during setup to eliminate any warp that the board has developed to that point in the process. Warped sections of the board were incurring a large quantity of holes with burrs when drilled.

Copper plating was the most difficult task in the plating category. In fact the plating tank that is now in use was designed around the MIB. Prior to the new tank the knee to center ratio was 3:1 and it is currently 1.5:1. Although the 8 mil board laminations were introduced at about the same time as the new plating tank and it is difficult to quantify the input of each element, the results from the standpoint of the MIB user are most acceptable. The most significant wave soldering improvements occurred following the introduction of the 8 mil laminations processed in the specially designed copper plating tank.

Two closing vendor notes: first, the improvements implemented to process the MIB have been used to enhance other processes at the vendor facilities from inventory control techniques to solder mask applications; second, fortunately for the MIB users while one vendor was having difficulty in delivering a product the second vendor was shipping one or two boards in acceptable condition. Eventually the situation would reverse and the cycle would begin again.

WAVE SOLDER PROCESS DEVELOPMENT

In addition to the challenges provided by the boards and the vendors the wave soldering process for the MIB was beset by its own problems. First was finding a machine that could accommodate a board as large as the MIB, and a machine that could supply the parameters needed to wave the board. Finding a machine that could supply sufficient preheat temperatures was typical of the earlier problems. Second was finding tooling boards that could be used for wave solder development. The third problem dealt with the frequency of having to reset the limits on many of the parameters when board material and machine changes occurred.

The Wave Solder Machine

The first wave solder machine used was a highly modified oil intermix that appeared to have been built in the early 16th century. Previously used for many development projects this transfigured unit never generated the preheat temperatures or a wave height sufficient to fill the holes adequately and yield never reached 50%. The second wave solder machine utilized was of fairly recent manufacture and belonged to a sister division of the company (located 40 miles away on the east side of Tampa, Florida). This machine was a fairly up-to-date unit with few drawbacks, but following a 6 month process development the sister division and the machine were sold off and were no longer available for wave solder.

The wave machine finally chosen to solder the MIB was located just across the division's own campus and, until the MIB, had been used exclusively for one other product. Originally the machine was thought to be inadequate for the atypically sized MIB because it was a bottom of the line unit of the supplying company and though it was only 2 years old it had already acquired a history of marginal dependability. Following several frustrating attempts to wave a tooling MIB, and very little support from the supplier, the development team began an upgrade program on the machine that lasted two years. Because of a series of problems initially encountered with the wave machine the speeds and temperature readouts from the machine were considered worthless and each parameter was triple checked by independent means. The machine's microprocessor was replaced, each of the conveyor fingers was replaced with a different configuration and held to a tighter dimensional tolerance. The solder pump was rebuilt from top to bottom including new belts and motor, upgraded impellers, bearings and lubrication system. Preheater electrical contacts were replaced as well as the entire fountain assembly which had warped to a point of losing 20-30% of the pumped solder between seal surfaces. Gasket material for the fountain assembly was upgraded, new replacement baffels were designed and built to generate the desired wave characteristics and the maintenance and calibration schedules were completely revised.

With each change came some improvement, sometimes a little, sometimes a lot, but slowly control of the process became a possibility. The situation involving all of the wave machine trouble actually put the development team into a more clinical mode, and maybe some paranoia resulted, but the end products were a top quality board and a very dependable wave solder machine.

Tooling Boards

Experimental tooling boards constituted the next priority. The team never seemed to have the board quantities necessary to properly assess all the variables, consequently each run was carefully planned to maximize necessary output. There were many scrap boards available but few MIB's with adequate plating that would solder. Boards for wave solder process development had to be scrapped solely for misregistration or other non-plating imperfections. Determining which soldering anomalies were process oriented and which were MIB related began as an art form because it was impossible to establish without a destructive test* whether problems were board or wave process related. Early in the development the process was constantly suspect as the cause, but in depth testing ultimately associated the majority of problems with the board. Coupon testing became an inconclusive indicator. Floating coupon pth's on solder at 3 different temperatures may normally indicate an acceptable board (when the coupons solder), but board performance did not match coupon performance in this case. The development team has found that on the MIB that copper and tin lead plating can be acceptable on the periphery of the MIB and totally unacceptable in the center. Unfortunately, the vendors have resisted all attempts to develop center coupons due to their center hole cutting procedure. Since each tooling MIB was soldered/resoldered 5 times to establish the maximum number of wave and temperature parameters, destructive testing was not an option and it became a priority to receive tooling boards with solderability potential as high as possible.

* Cutting and removing any portion of the board for analysis was ruled out in an attempt to keep the tooling board as close in configuration to the flight board as possible. Total mass was considered an important criteria.

Parameters

Finally there was the problem of redefining and/or proving the parameters initially set on a board with one type material for use on boards with the next material. At best, the existing parameters could be proven functional on the next level of material. Use of existing data was always attempted first in each material transition. At worst, the parameters would have to be redefined and usually one change would ripple through the process to affect other parameters. For example, if test running a new material with previous parameters generated an unacceptable board* due to insufficient heat as many as 5 other parameters had to be checked to determine if new settings were required. Insufficient temperature might require: full MIB temperature studies, prebake oven adjustments, conveyor speed changes, upper and lower preheat checks and solder temperature studies. Preheater studies were further complicated by the use of from 1-3 available banks of preheat on the wave solder machine. It was eventually determined that utilizing all three available preheaters on both top and bottom produced the best results for all the materials run; an even distribution of heat across the board was as important as the total amount of heat.

Each tooling board wave soldered included a soldering sample of 5-6 connectors mounted at various points along each of the 2 channels of the MIB. Any remaining unsoldered connector joints were masked off for future runs.

A simple pattern shown in Figures 2 and 3 was used to track the performance of each connector position on the MIB and to track overall board performance for any resultant accept/reject patterns. For instance, if a series of pins of each connector along one edge of the board showed poor or no fill (reference Figure 2) or the ends of each connector toward the center of the board indicated poor fill (reference Figure 3) it was considered a plating problem or a non process related problem. Conversely, connectors that showed poor fill along the "D" row (reference Figure 4) when rows A, B and C filled relatively well were known to be process problems and almost always related to insufficient temperatures. However, when a connector such as the one shown in Figure 4 was flanked on both sides by fully filled holes at virtually every location the trouble would inevitably be traced to poor plating.

Connectors were reused whenever possible. At $200 + for each connector they became almost as precious a commodity as the tooling boards. A method was developed to run a fully tested and spent tool board across the wave reflowing the joints, allowing for removal and salvage of the connectors for reuse. Early in the development of this method several tooling boards and some connectors were damaged beyond repair, but the salvage process ultimately evolved into an excellent routine in which all the components were salvaged and reused. A safer technique has since been developed for connector removal that does not require operators to work in such close proximity to a wave. While this new method was primarily developed to reduce rework time on flight MIB's, it has also been used to retrieve connectors from tooling boards. The newer method is somewhat operator dependent (it takes substantial practice to consistently achieve good results) but a connector can be completely reflowed, removed and pth's blown clear of solder in less than a minute. Processes such as this that were invaluable at one time are rarely used on flight MIB's today because yields are 99.8% and increasing.

* Where an unacceptable board had a yield of less than 90%, there are a minimum of 1,000 unacceptable solder joints that could require over 30 shifts to rework.

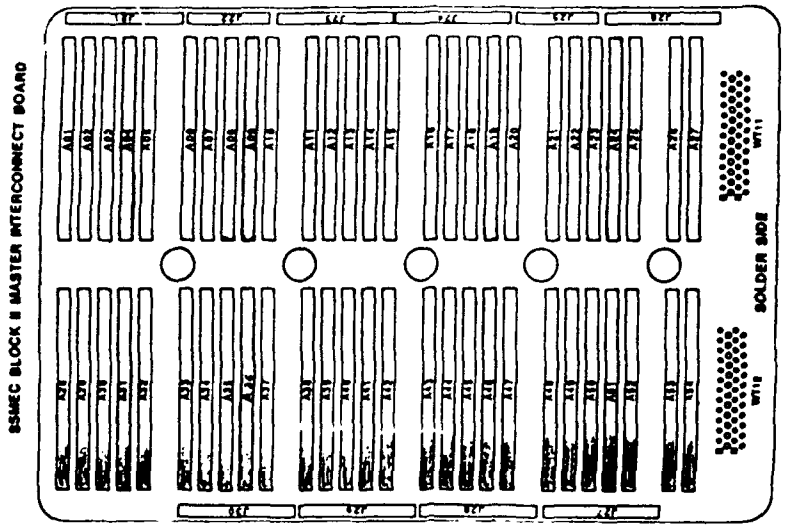

FIGURE 2. POOR SOLDERING
ALONG AN ENTIRE EDGE
INDICATED PLATING PROBLEM

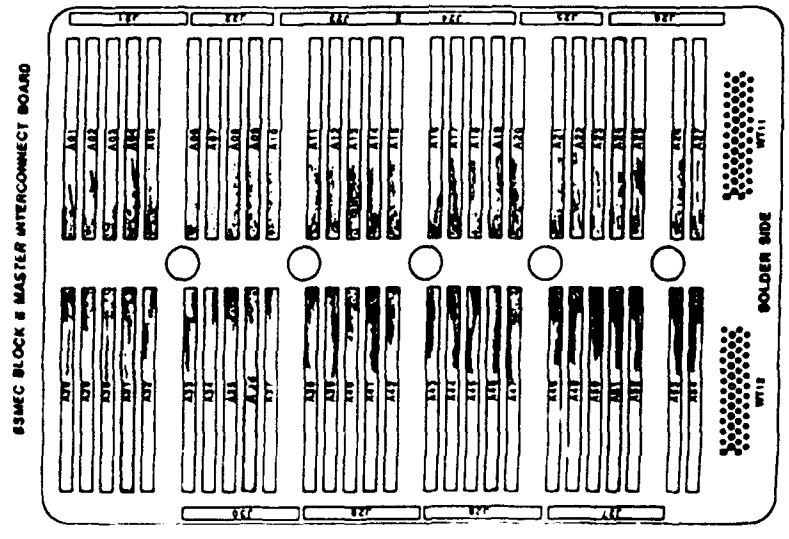

FIGURE 3. DEFECTS HEAVY AT THE
MIB CENTER AND TAPERING ALSO
INDICATED PLATING PROBLEMS

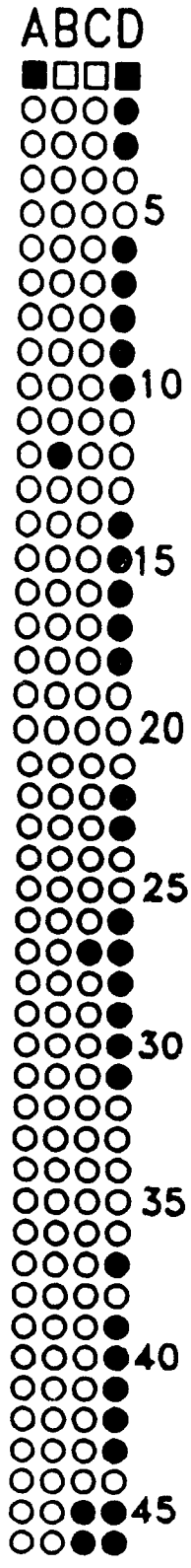

FIGURE 4.
PROCESS PROBLEMS WERE MORE LIKELY TO TAKE ON AN INDIVIDUAL CONNECTOR PATTERN. TYPICAL IS THIS REJECT SHEET INDICATING THE "D" ROW TO BE SIGNIFICANTLY WORSE THAN THE OTHER 3 ROWS.

THE CURRENT PROCESS

The main wave solder team consists of a group leader and 2 operators supported by a test technician from the Environmental Lab monitoring temperatures. The same people are used for the wave solder every time and if one of the team is not available for a scheduled wave the wave will be rescheduled rather than introduce a less experienced operator. There is a production engineer, a quality engineer and a DCMC representative present during each wave soldering of a MIB. Most wave soldering is witnessed by a customer representative as well. The team constantly backs each other up going over and over each step of the setup and process to insure every step is complete and to insure, ultimately, a top quality board. Knowing how to complete each step, when each step needs to be completed and getting each step completed consistently is an advantage the MIB has that should not be undervalued. The more intricate the process became more emphasis was placed on keeping the team together. Repeating the process with the same individuals, board after board cannot be emphasized enough and has proven its advantages.

The current MIB process is a 4-step operation consisting of board preparation, wave solder, inspection/rework and final assembly.

Board preparation begins with visual inspection for surface defects, coupon soldering test, dimensional checks and electrical tests for shorts and opens with emphasis on high resistance shorts. The board is then marked with the appropriate part numbers and serial numbers, the markings are coated and two drillouts are completed to isolate circuits. While the board is being prepped the connectors are inspected for body and pin damage, bent pins and proper identification, but they are primarily checked for the proper number and configuration of the 5 socket wires in the female/receiving side of the connector pin. Incomplete sockets have been somewhat of a problem in the past. The pin sockets are covered with tape to avoid handling damage whenever the board is not in bakeout or submerged in a cleaning solution. The connectors are then tinned, baked and assembled to the MIB with tooling hardware that is bonded in place. Flight hardware is difficult to position on the wave machine conveyor and unbonded hardware has fallen off prior to wave soldering creating additional rework. The MIB and connectors are then "slosh" cleaned (in a custom tub* that continuously moves the fluid over the assembly board) in tricholorethane for thirty minutes and then in a solution of isopropyl alcohol and DI water for an equivalent period. The assembly is then submerged in a second solution of isopropyl alcohol and DI water and checked for ionic contaminates. Excess fluids are blown off the board and the assembly is vacuum baked for 18 ± 2 hours at 95 ± 5°C at a minimum of 74 cm Hg. The length and temperature of bakeout were originally established based on the difunctional board material with a safety factor added. Early in the process development when vendors were having plating problems, bake out was extremely important for reduction of moisture in the laminate and the resultant blow holes at the weak points in the copper barrel. The vacuum bake parameters have not been updated as board revisions occurred.

Following vacuum bake the MIB is fitted with eight thermocouples which are used to monitor board temperatures during two operations in the process, once at wave solder then again when the MIB is in rework. The thermocouples are a 0.030 inches diameter type T with quick-disconnects attached. The welded ends of the thermocouple are held in their

* The board lays flat in a stainless steel tub covered with fluid. The tub is fitted at one end with an eccentric wheel driven by a low voltage motor that raises and lowers that end of the tub.

place as close to the board surface as possible with dental cement. The perimeter of the cement where it contacts the board is covered with epoxy to keep the cement from lifting off during the trichloroethane baths. The thermocouple wires are cut 15 foot long which allows for the length of the wave solder machining and feed length to the data logging device.

The MIB is then masked in preparation for the wave soldering operation. The larger areas are masked with one inch wide Kapton tape and the smaller areas with a latex based high temperature flexible mask that requires an approximate 60 minute air cure time. Kapton was chosen for its excellent adhesive characteristics and high operational temperature: limits are from -100°F to 500°F with short exposures to 700°F. Initially, polyester film tape was used but was discarded quickly when the tape caught fire in the preheat area of the wave solder machine setting off the halon extinguishers and catching the immediate attention of the local fire department. Masking tape was also tried on several boards but leaked solder regularly around the edges and discolored to the point that the process was obviously pushing masking tape's kindling temperature to the limit. A note of caution about Kapton tape is that it does contain silicone and is not conducive to use as a masking agent in conformal coating operations.

The final board preparation for wave solder is the addition of a wave solder dam that follows the complete perimeter of the MIB. The dam is constructed of stainless steel Type 303 that is 0.190 inches thick for strength to combat warping as it is exposed to the heat but has panels milled out of the sides and ends to reduce the weight. There are (5) 3 1/4 x 1 1/4 inch sections on each side, (2) 5 1/2 x 1 1/4 inch sections on the end plate and (2) 5 1/2 x 3/4 inch sections on the front that have been milled out for weight loss. Thickness of the dam in the panels is 0.070 inches. The dam stands 1 1/2 inches high and has 4 slots cut from side to side along the front to help determine solder height during wave. Wave depth was considered an important input in the early stages of the process development but is no longer monitored (input gathered using a glass plate for wave symmetry has replaced the need for wave depth input). The dam is held in place on the board by 10 bolts: 4 along each side and one in the middle of each end. At any point where the mounting hardware for the dam can damage the board surface that area is protected with a piece of Kapton tape. The rear plate has a strap with two finger tight hold down screws to control the movement of the eight thermocouple wires. The meeting surfaces of the board and dam are sealed along the outside edges with 1 inch wide Kapton tape to eliminate any chance of solder leaking onto the component/connector side of the board. In addition to keeping the solder from the wave off of the component side of the board it also protects the top surface of the connectors when the board is laid flat with the solder side up during the fluxing operation. The dam protects the flight board from contact with the setup board and the oven walls during the prebake operation and allows a margin of safety when the board is set on its side during a pre-flux cooling operation. Due to the width of the dam the board with the dam attached can stand on its side without assistance. While operators are instructed to maintain constant contact, the dam allows some margin for emergency situations when that operator-board contact might be interrupted.

THE SETUP

The MIB is now ready for wave and is wrapped in bubble wrap and transported to the wave solder room in a building across campus. The first check prior to wave soldering is the specific gravity of the RA flux. The specific gravity is to be 0.880 ± 0.015 as read from a standard hydrometer at $71° \pm 2°F$. The specific gravity test is valid for 4 hours, if the flux tested has not been used within that period the test is repeated to insure that inputs to the process have not changed. Fluxing is accomplished using a hand pumped spray bottle and a 1 inch wide brush with undyed hog bristles. The spray bottle is graduated from 300 to 425

grams along the side of the bottle, and is filled to the 410 gram mark. Ten grams of flux are then pumped through the spray nozzle to insure that the nozzle has been cleaned and adjusted properly. The spray bottle is used only on the MIB and isolated after each use. Flux from the bottle is never reused from one MIB to the next and the brush is discarded after each MIB is wave soldered. Flux usage is at 85 ± 10 grams sprayed and brushed evenly across the MIB's solder surface.

The next item that is checked is the solder in the pot of the wave solder machine. Solder samples are pulled every 10 turn-on days which approximates a 3-4 week calendar period. The samples are sent to an off campus laboratory for analysis, an analysis which includes percent tin/lead (63/27 respectively), and percent trace elements by weight and contamination of any kind if found. The analysis is geared to verify acceptance per QQS-571e. A copy of the analysis results must be available for the MIB package and appropriately dated (within 30 days of the last analysis logged in or no earlier than the first in the series of the last 10 turn-on days).

Next the oven data logs are reviewed to insure the required vacuum bake has been completed. Following the 16 hour vacuum bake when the board was "slosh" cleaned every effort is made to keep the MIB in a storage oven to minimize the moisture absorption time (time when the MIB is exposed to room temperature and humidity). If the moisture absorption time reaches sixteen hours the MIB must repeat the 16 hour vacuum bake. Once the bake out has been verified the MIB is placed in a storage oven at 55° ± 5°C.

Machine setup is next and begins with the removal of the mechanical fluxing devices, foam and/or wave. The conveyor width is then set to accommodate the MIB. The setting at 14.7 inches reflects a relative measurement between 2 points along the conveyor rail and not the actual distance between the 2 rows of conveyor fingers that actually hold the MIB. Initially the fingers were bent both to and from the conveyor chain making the measurement inconsistent and due to conveyor speed problems the conveyor was usually moving, which added to the difficulty of accurate measurement between fingers. Although the finger problem has been corrected, the conveyor speed problem persists and for that reason use of the original measuring technique continues. Thus, a relative number between two stationery points was established. The solder pot temperature is then set to 500° ± 5°F, this is set 3 hours before the planned run time to insure the pot will stabilize at the desired temperature by the scheduled wave solder time.

Preheaters are next on the checkoff list and have provided some problems throughout the process development. The infrared preheaters thermally condition the MIB prior to soldering and consist of three banks of heating tubes which may be switched independently. The tubes run parallel to the conveyor travel and are set at 600° ± 10°F. The preheaters are turned on one hour prior to the planned wave solder time. The conveyor housings which slide open in a telescoping fashion to either end of the machine are fully extended while the preheaters come up to temperature and stabilize. Historically, maintaining the board temperature profile through the preheater stage has presented its challenges, including heater sections that switch off, exhaust vents that vary in their cfm delivery and air conditioning outlets that vary in their output temperature. Early in the development some tooling boards were showing randomly insufficient solder along the left outboard edge (the preheater banks are numbered 1-3 from right to left facing the loading end of the machine). After some fruitless process alterations the board was dissected and the plated through holes were found to be of the same quality throughout the board. A thermocouple was mounted to the left outside edge and on the third trial run that extra thermocouple indicated a significantly lower temperature than the temperature at the center and to the right of the board. Insufficient preheating explained the

poor soldering and eventually the problem was traced to an inadequate power transformer that, due to a lack of capacity, intermittently triggered a shutdown of the third bank of preheaters. The transformer was upgraded and the problem has not reoccurred, but to this day a thermocouple remains mounted to the leading left top side of the board and is monitored for significant temperature variance. Prior to wave soldering, all three banks, top and bottom, are monitored visually to insure a full "ON" condition. This problem was new to this machine because all of the previous boards soldered on the machine were narrow enough to require the use of only 2 banks of heaters. The MIB's width required the third bank of preheaters that overloaded the poorly "spec'd" transformer. Early in the process development, when board materials made temperature profiles through preheat much more difficult to control, one variable identified was the air conditioned temperature of the wave solder room. Room temperature varied as much as 10 degrees F and eventually the single supply vent was closed off completely one hour prior to the planned MIB wave solder. The wave solder facility has since been remodeled and use of the more temperature stable polyimide material has minimized this earlier problem. A potential problem was averted when one of the MIB team members noticed an unusually high level of noise at the exhaust vents of the wave solder machine. Investigation found a 50% increase in the cfm of the machine exhaust.This increase was due to a design change made by another product user of the wave solder facility without the knowledge of the MIB wave solder team. The change had the potential of running the MIB too cold by pulling too much ambient air across the conveyor. Following this episode all users of the wave facility sat down together and set up procedures for maintaining the machine with all users cooperation and awareness of changes. Inevitably, disaster or near disaster produced a necessary reaction. Only heads-up awareness on the part of a MIB team member saved a dramatically expanded rework effort.

The next parameter to be set is the conveyor speed, regulating the time the MIB is in preheat and the length of time the MIB is on the wave. The conveyor speed has always had its problems/eccentricities, the worst of which was going from a set level to a dead stop for no apparent reason. This problem was traced to the previously discussed power transformer. Once the transformer was upgraded, the problem was virtually eliminated. The conveyor has realized one unexpected stop with the new transformer but the difficulty was quickly diagnosed as a calibration problem and tuned out. Two other persistent problems have been the inaccuracy of the machines digital readout regarding conveyor speed and the length of time required for the conveyor speed to stabilize once it has been set. Although the machines digital readout of the conveyor speed is incorrect, it is consistently incorrect by 7% and does not respond to any level of calibration. Fortunately the error which occurs for every setting is a constant value and is predictable and reliable for a specific setting. For every MIB wave soldered the conveyor is set and checked at least twice with a stopwatch after the conveyor speed has stabilized to insure the conveyor is running at the desired speed. Currently, to attain a 1.875 feet per minute conveyor speed the machine is set to 1.75 feet per minute and the actual speed does not vary more than ± 0.01 fpm from the desired 1.875 fpm. The only time sufficient variance occurs is during the 3 minute period following conveyor "power on" when the conveyor speed is stabilizing. During that 3 minute period the variance can be ± 0.2 fpm and change rapidly from a relatively fast speed to a slow speed. A safety factor of two additional minutes is allowed and there are no readings checked by stopwatch until a full 5 minutes has elapsed following conveyor start up.

Finger height is the next parameter set. Finger height is the distance between the bottom of the conveyor fingers and the highest point along the solder pot and fountain. The measurement serves a dual purpose. First, it functions as a control point to eliminate contact between board components/connector pins and the solder pot. This condition can

significantly increase the dwell time of the MIB on the wave, which can, in turn, ultimately result in board destruction. As the process was being developed, the team occasionally noticed that the MIB would stop while over the wave and had to be manually moved forward. Review of this intermittent problem showed that a portion of the connector pins extending below the lower board surface would contact the highest point of the solder pot obstructing the forward progression of the MIB. The obstruction was to the point that the conveyor fingers continued to move under the MIB sliding along the board edges while the MIB remained fixed on the wave. The team was aware of the following three facts: that there were two different connector pin lengths, that the machine had been set up for the longer pins and that all other parameters remained unchanged. It took two additional runs to determine that the problem was the varying length of the conveyor fingers. The variance in finger length was as great as 0.100 inches had never affected other boards run on the machine because they were too short to be affected by the difference in finger height. The leading edge (or one side) of the MIB could be as much as 1/8 inch lower or higher than the trailing end (or other side), and the condition occurred randomly. Frequency depended on the position of the longer/shorter fingers on the conveyor as the board was loaded. The majority of the board runs were normal, but the process was never consistent or dependable. Two new complete sets of fingers were ordered. While awaiting delivery of the new fingers the existing fingers were removed, measured and color coded by length and then reloaded to the machine in a fashion that had all the short fingers in a group on corresponding sides of the conveyor and in a long enough string to accommodate the MIB. An attempt was made to bend the errant fingers into a usable shape, but the distortions were greater and more uncorrectable than the original configuration. This revised finger arrangement had its problems. One problem was that once the height had been set for a particular set of fingers, the board had to be loaded on that color group. Placing the board on any other set of fingers put the board position too high or too low relative to the wave and that generated excessive rework. Timing also became a problem. Waiting for the appropriate fingers to reach the board loading point on the conveyor had the potential of both hot and cold loads. If the board cooled too low prior to the correct fingers arriving at the load position the MIB was returned to prebake and the process restarted. The cooling rate and time, and the fluxing time were calculated and totaled for the MIB being run. Based on the travel rate of the conveyor, a point was located along the conveyor rail and when the first finger of the appropriate color section reached that point on the rail the MIB was pulled from the prebake oven. When the MIB cooled to the proper temperature and had been fluxed the correct fingers would then be in position on the conveyor for loading the MIB. Upon arrival of the new fingers both sets of new and the original set were merged, measured and produced one full set of fingers with lengths that were within 0.018 inches from the shortest to the longest finger. This limited variance in finger length proved to be an effective solution to the problem. The board could be loaded at any point on the conveyor and the solder results remained unaffected.

The second purpose that the finger height measurement serves is to determine the depth of the board in the wave. After the finger length and the corresponding board height had been corrected a second breakdown became evident when the board would not achieve the necessary submersion in the wave. This submersion deficiency was probably masked by the finger problem. Even at the lowest possible finger height setting there were runs where the board would only achieve 60% of the desired submersion. With the thicker boards that were being processed at the time (0.270 inches thickness) the maximum submersion was the goal and ranged from 125% submersion to an estimated 150%. The problem was resolved temporarily after each machine maintenance where the solder fountain and pump assembly were removed, cleaned and reassembled. The machine maintenance was doubled over the original schedule, but eventually, during a run just after the routine maintenance had been completed the wave failed to reach its expected height. The solder fountain assembly was removed and a gap was observed along the flange of two sealing surfaces.

This gap that had not been detected during the reassembly procedure. Filled with a high temperature malleable gasket the problem was corrected, but returned following two additional runs. A new solder fountain was ordered and the gasket material changed to a carbon fiber composite 0.120 inches thick. Using a 10 turn-on day maintenance schedule and the new parts the problem has not reoccurred.

Following a formal wave solder class at an offsite, the team decided to check the symmetry of the wave. Symmetry check started with a premarked 8 X 10 inch allegedly tempered glass supplied from a vendor as an over the counter item. It was later decided to determine exactly what the MIB was "seeing" as it crossed the solder wave and a piece of tempered glass was ordered, the exact length and width of the MIB (including the radius on the corners). The glass had to be a minimum of 0.250 inches thick or it would shatter on the wave. The team marked the glass using one inch wide kapton tape and spacing the tape marks 1/2 inch apart from side to side down the length of the glass. A temporary dam is taped to the glass edges and a light coating of flux is sprayed on the solder side. While the glass runs over the wave it is easy to insure full coverage from side to side and count the inches the board will "see" from the leading to the trailing edge. The overall pattern of the solder against the board can also be observed and if appropriate the necessary adjustments made. Prior to this positive symmetry check a great deal of time was spent attempting to level the machine, the solder pot and the solder fountain in an effort to achieve an even flow of solder from side to side and front to back, and provide each point on the MIB with an equal exposure to the wave. The leveling process produced little confidence that the wave was equal across the board surface and could never be verified. The glass on the other hand provided a positive look at what was happening to the MIB and generated a great deal of confidence. The glass can be stopped on the wave and the wave pattern observed in a semi-static mode, but after several seconds the wave pattern begins to distort generating a tail along the trailing edge. Restarting the conveyor repeats an accurate pattern. With the thicker boards the pattern was complete side to side and measured four inches front to back. The thinner boards achieve outstanding solder results with a full side to side pattern and only three inches of solder front to back.

Being able to observe the wave pattern made the adjustments to the finger height and the lambda (wave height) control much more efficient and accurate. With the thicker boards the lambda setting at the early stages of process development was set at the pump's maximum, 2000. The number is relative and does not bear a direct correlation to pump speed, cm^3 of solder pumped, etc. The thicker boards seemed to require all the solder that could be pumped to generate an acceptable yield. The lambda for the current boards is 1500 or 75% of the original setting and provides excellent results.

Several other minor checks are made prior to wave soldering a flight MIB but these checks are responses to problems of singular occurrence. Examples would be checking the solder height in the pot and checking the front and rear plates of the solder fountain for the proper position. A cursory check of the flow control plate is also completed (this plate allows minor adjustments to wave height). With all of the above parameters set, checked and rechecked it is time to run the MIB over the wave.

THE WAVE

Waving the flight board begins with the flight MIB being removed from the prebake oven and a dry run is completed to insure there is no interference with any of the solder machine parts. Without preheat and the solder pump off the flight board is loaded onto the conveyor which is a check that the proper width has been set. The flight board is allowed to progress the length of the conveyor and the clearance between the connector pins and the

solder pot and fountain is visually verified to insure no hang ups will occur during the solder run. The flight board is returned to the prebake oven and positioned behind the setup board. The oven is turned up to 240°F* and the boards remain in prebake for one hour for the purpose of stabilizing the interior temperature of the board. The thermocouples on the setup board are connected to the temperature recording monitor. When the prebake session is complete the setup board temperature readouts are checked. If they are within 5°F of the oven temperature, the setup board is removed from the prebake oven to the fluxing station and set on its side to cool. The setup board has 4 thermocouples: one on the top leading edge center (designated "No. 1"), a second is mounted center of the board solder side, a third on the leading edge and to the far left top side and the fourth at the center of the trailing edge and on top. When the No. 1 thermocouple reached 190°F a moderate amount of flux is applied to reduce the amount of solder that adheres to the masking agents. The connectors on the setup board are completely masked off so that board can be reused. When the No. 1 thermocouple indicates 170°F the setup MIB is loaded to the conveyor. Because there are only 21 inches of clearance at the beginning of the conveyor the board is loaded with the leading edge already in the preheat section. The preheat section is two feet long and allows the board to reach 245°F. There is a ten inch gap between the end of the preheaters and the front of the solder wave, and the board can cool from 10-20°F. As the leading edge of the MIB touches solder the goal is to have the No. 1 thermocouple reading 230° ± 5°F. That range produces an excellent yield. If the setup board fails to meet any portion of the temperature profile the setup board is returned to the prebake oven and the failure investigated. Adjustments are made and the setup run is repeated until the temperature profile is correct. The technician from the Environmental Lab calls out the readings of the No. 1 thermocouple to the production engineer who is visually monitoring each step of the process. The callout relieves the engineer of attempting to monitor a temperature display and concurrently monitoring the MIB activity. If the run of the setup board is successful the thermocouples of the flight board are connected to the monitor. Following two consecutive readings of the temperature indicating 235°F or higher for each thermocouple the board is removed from the prebake oven. Of the eight thermocouples on the flight MIB 4 are placed in identical positions as the setup MIB with 4 redundant as a safety margin for both the wave solder operation and the rework operation. The flight MIB is set on its side until the board cools to 190°F. With the MIB now laying flat and the solder side up, flux is sprayed onto the MIB by one operator while a second operator brushes the flux uniformly across the surface. Both operators are wearing a respirator due to the volume of volatiles generated by the flux applied to a 190°F surface. The technician monitoring the thermocouple temperatures is calling out the No. 1 value every 12 seconds (the time it takes the data logger to channel through the eight readings). When the board reaches 170°F it is loaded solder side down on the conveyor. The second operator monitors and calls out the position of the board on the conveyor. "Loaded", "full preheat", "exiting preheat", and "in wave" are written on the temperature printout by the technician at the monitor. The positions are posted next to the appropriate time and temperature when the callout was made. This time, temperature and board position were invaluable in developing the process and diagnosing temperature problems. Currently, the temperature profiles are identified and filed for failure analysis if required.

The group leader is always in a position to shut the wave, preheaters and/or the conveyor down on command of the production engineer. The production and quality engineers are monitoring the process for anomalies and to direct the appropriate action. If

* The oven heats from the 130°F storage temperature to the 240°F wave solder temperature within seven minutes.

the temperature profile is appropriate the board is allowed to solder; if the profile is off the wave is shut down, investigation and adjustments are made and the setup board is rerun. If the profile on the flight board cannot be met in two consecutive tries the run is scrubbed until proper corrective action can be determined. After the board completes the wave it rides to the end of the conveyor, the conveyor is switched off and the board is allowed to cool for 5 minutes. The board is moved to a work station where the masking and solder dam are removed. Once the board reaches room temperature the MIB is placed in a vapor degreasing tank of heated trichloroethane to release the remaining flux from the surfaces of the board and the connectors. The board is rewrapped and returned to the Final Assembly work area for the remaining operations.

Following the vapor degreaser cleaning which removes the majority of the flux residue from the board, the MIB is "slosh" cleaned for 36 hours. First with (2) 12 hour trichloroethane baths in between which the fluid is changed, and (1) 12 hour alcohol-DI water bath. The baths remove the remaining ionic contaminants. This is verified by a MIB submersion test for ionic contamination. The excess fluid on the board from the test submersion is blown off the MIB and the MIB is vacuum baked for 16 hours.

There are two types of connectors soldered to the MIB. The "A" body connectors are wave soldered to the layer 22 side of the board (topside) and the "J" body connectors (or edge connectors) are hand soldered to the layer 1 side of the board. To hand solder the "J" connectors a hot plate fixture is used to achieve and maintain the board at a solderable temperature level, from 170° - 190°F. The hot plate fixture also serves as a rework station for improperly soldered joints, rejected from both the wave and hand solder operations. The hot plate fixture was specifically designed around the MIB's size and for the MIB's temperature requirements.

Redundant temperature controls eliminate board and fixture overheating. The temperature of the hot plate fixture itself is monitored by two separate controllers: the first is used in a thermostatic capacity and is used to set the desired hot plate temperature and hold that temperature within a range. The second controller is strictly an over-temperature monitor that interrupts power (at some preset limit) to the fixture until the controller is manually reset. Any violation of the top end limit is signaled by both audible and visual alarms.

The MIB is monitored by an eight channel data logger which serves 3 functions. The primary function, completed by five thermocouples mounted to the bottom side of the board, is to monitor temperatures at various positions on the MIB and signal the controllers for a power interrupt if the MIB registers a temperature that exceeds input limits. The second function provides operators with inputs regarding board temperatures, allowing the operators to rework and solder the MIB at optimum conditions. The third function is to provide a temperature profile for each board and a temperature history for each fixture. This background data provides a basis on which decisions can be made to problem solve, to determine corrective actions and to adjust temperatures in compensating for variables in board characteristics. The temperature value of each thermocouple is printed every ten minutes that the board is on the rework fixture giving the date, time, and the eight temperature values.

Due to high temperature and the length of time operators are exposed to fixture and board heat, and evaporating flux volatiles and trichloroethane, the fixtures and surrounding work places were designed to minimize the effects of the process. A combination of thermanesthesia materials (phenolic and marinite) and high fixture sidewalls was utilized to

eliminate skin contact with hot board/fixture surfaces. Burns had been a serious problem early in the process development while using a conventional hotplate. Finally, exhaust hoods were placed at the rear of each fixture. These remove fumes generated by evaporating cleaning solvents and various soldering agents.

The "J" connectors are mounted to the board with flight hardware and hand soldered using an iron with a tip temperature of 750°F and feeding 3.75 inches of 0.010 inch diameter solder to the hole. There are two types of "J" connectors. Eight of ten "J" connectors have 120 pins each and the remaining 2 have 68 pins each.

The tooling hardware used to hold the "A" connectors in place during wave solder is replaced with the flight hardware and the board moves on for a survey of the solder quality.

Two inspections take place to determine the quality level of the solder joints on the board and to identify which areas of the MIB will require rework. First is a visual review of the solder joints, all 11,642 of them, which is completed using a 5-10X scope viewing the layer 1 or solder side of the MIB. Typical points of quality are surveyed, e.g. discernible leads, bright and smooth solder surfaces, the absence of pits, holes voids, cracks, bridging, etc. Quality is measured against the standards set forth in NHB5300. If visually discernible defects are found each is plotted on a map. Each connector has a corresponding pin location guide similar to the one shown in Figure 4. Any pin identified with a defect has the corresponding circle filled in and the type of defect is identified in writing next to the filled circle. When running the thicker boards early in the process development the dwell time on the wave and the depth in the wave were necessary in filling the plated through holes. With parameters set to fill the pth's the resultant visual defects were excessive (as many as 2,000 on a board), but visual defects were the lesser of two evils. Unfilled or partially filled pth's were time consuming and expensive to rework and required the MIB to remain on hotplates for too long experiencing heat levels for periods of time that were not desirable from either a quality or end performance standpoint. At times, the effort was so intense that following repeated efforts to wick out pth's the pads would pop off the board surface or just fade away. Soldering iron to pad time must remain minimal for product survival. Visual defects require less hot plate time and less iron-to-pad time than plated through hole rejects, for that reason the wave solder parameters are set to fill the pth's first and work the visual defect problems second. Once the pth yields were consistently over 98% studies were made on reducing the visuals or solder side defects. The results of the studies were implemented and are a permanent part of the current process. Visual defects have been reduced over 50% to an acceptable, but not an ideal, level. Reducing the visual defects was accomplished while increasing the pth yield to a consistent 99.8% +. Efforts continue to reduce the visual defects and the associated rework cost.

The second board review for defects is for plated through hole fill and is accomplished using a microfocus x-ray system. Visual inspection of the top sides (connector sides) of the solder joints is virtually impossible. Due to pin rows 4 deep and full pin encasement by the connector body, top side inspection is partial for the outside rows and non-existent on the interior rows. Inspection therefore, is accomplished using a computer enhanced real time x-ray image. The microfocus x-ray unit allows on line viewing via a television screen with optional photographs and video tapes for visual records.

Advancements in the design of x-ray tubes and digital processing technology have provided a method of MIB solder joint inspection. Labor technology and time consuming inspection of "hidden" solder joints has given way to a new "real time" review technique. Microfocus x-ray tube technology coupled with digital processing of video signals provides a real time inspection system capable of displaying enhanced x-ray images of visually

uninspectable solder joints to an operator via a CRT screen. With the addition of a manipulator to this system to hold and move the MIB, a real time image rotating and tilting gives the operator varying perspectives of the MIB, providing virtually three-dimensional viewing. Normal x-ray imaging using photographic film has several drawbacks. The film is costly to purchase and develop and can easily by marred by handling. Literally thousands of radiographs would be required to obtain the optimum angles and film exposures to complete a master interconnect board.

The x-ray acceptance criteria for MIB solder joints is as follows:

1. 100% hole fill is required. The intent of this criteria is to have a continuous solder column in the pth to support the connector pin.

2. Total internal voiding up to 45% by volume is acceptable. The sum total of all voids within a solder joint must be no more than 45%.

3. A partial fill with or without internal voiding is acceptable provided solder flow to the top of the hole is evident on one side of the hole.

4. Shrink back on the component side is acceptable provided it cannot be construed as a blow hole or a solder void.

Interpretation of x-ray images is subjective. To assist in the interpretation, schematic figures of acceptable and rejectable conditions are illustrated. Copies of these conditions are in Figure 5.

The microfocus unit provides the most important dimension of quality review.

Pth rework is accomplished using the MIB hotplate. This is the same hotplate discussed when reviewing the hand soldering of the "J" connectors to the board. Every operator that works on the MIB is trained, tested and certified before processing a flight level MIB. Plated through hole rework is a 2 step procedure: remove and refill. Removing the solder from a 1/4 inch deep hole that has a 0.040 diameter generates its own level of stress. With a 0.024 diameter pin permanently affixed in the hole and a lead extending from the only workable side, the task becomes extremely difficult and demands experienced, patient operators. While a general method of rework has been outlined, each operator is allowed their personal license to incorporate his/her exact methods for achieving the goal. Initially, a heat and vacuum desoldering station was tested as part of the MIB rework process but resulted in too many lifted pads and was abandoned. The result was wick only solder removal and a reiteration of the point that boards thicker than 0.220 inches generated added process difficulties. As the MIB's were received with 0.220 inches thickness and less, rework tended to be a more normal task. The heat-vacuum desoldering station was reinstated to the process, but only after several different brands had been evaluated. The current desoldering unit uses 100 psi house air pressure to drive a vacuum at the heated tip that is placed over the lead before the unit is activated. Success is an acceptable 75% of the solder removed and the remainder removed by wicking with a number 1 size fine braid wick.

Final assembly consists of hardwires soldered to surface pads where required. There are seven hardwires by design. The input cables are then soldered to the MIB, 2 cables with 62 solder joints per cable. The MIB receives a final inspection and is moved on to the next level of processes.

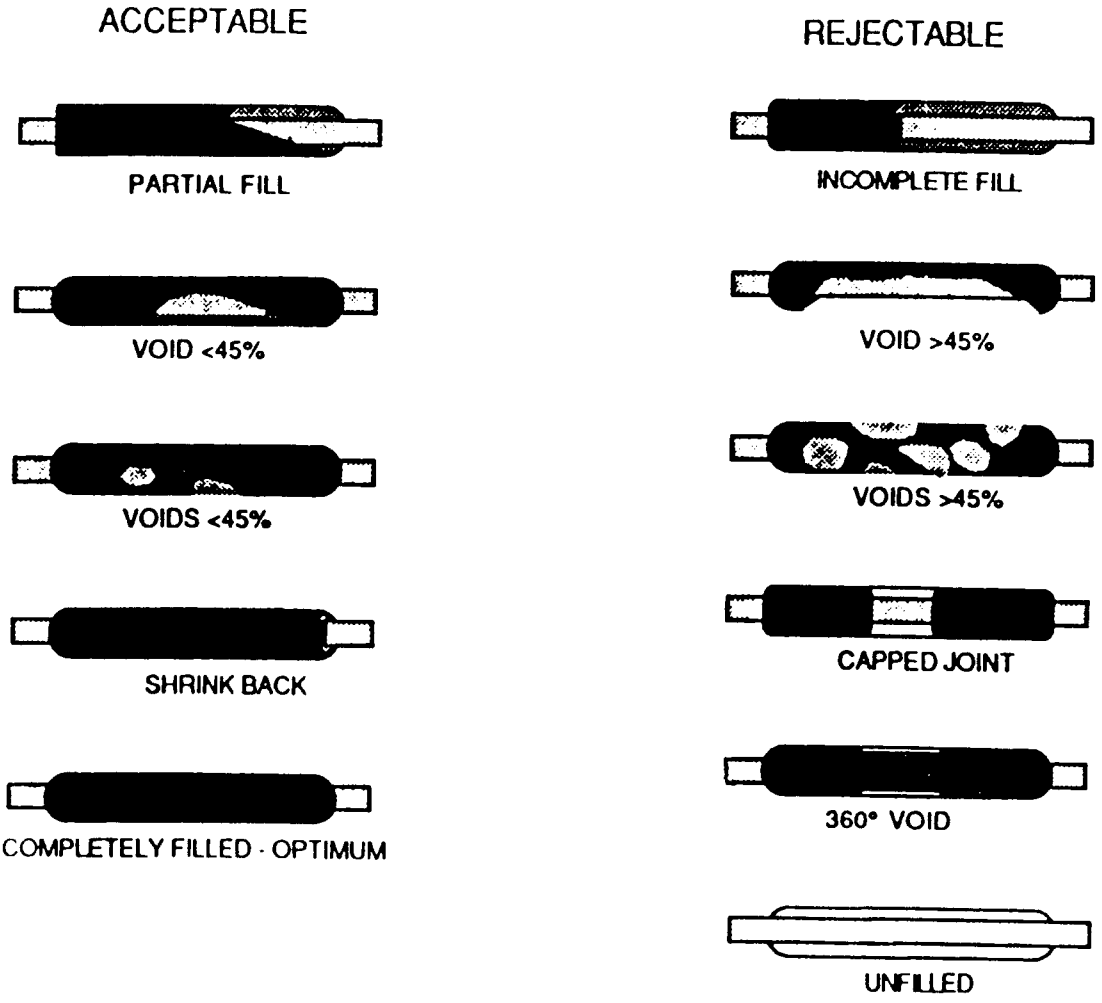

FIGURE 5

CRITERIA USED IN X-RAY REVIEW

Basically, if the MIB's were plated well they soldered well, similar to any other board - good input = good output. The team started out striving for plated through hole fill and is currently working to eliminate the visual defects that the MIB is experiencing. While it is somewhat difficult to process a board the size of the MIB, it certainly is not impossible. It is anything but routine, however, and does require a few specialty tools and some practice. Attention to detail seems to generate great dividends. What had been an undependable wave solder process with a yield of less than 50% has been refined to an extremely productive process with a consistent yield of 99.8% plus. Attention to detail, exacting specifications and a team that emphasized total quality involvement made it happen.

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Testing for Contamination on Electronics Assemblies Cleaned Using CFC-113-free Techniques

by

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ABSTRACT

This paper describes and discusses all the main methods for determining the presence of and measuring the quantity of diverse contaminations on cleaned electronics assemblies. The latest innovations in the field are described. As cleaning with CFC-113 and 1,1,1-trichloroethane (methyl chloroform) blends is phased out, other cleaning methods must be introduced or, in cases where reliability is of secondary importance, "no-clean" techniques, including controlled atmosphere soldering, may be used. Generally, all types of cleaning process should be regularly tested, i.e. followed by a contamination test, to determine whether the soldering/cleaning process remains within acceptable tolerances. Some of the less scientifically-developed fluxes and processes used with "no-clean" soldering techniques leave residues which may be classed as corrosive and dangerous under poor climatic conditions: this implies that process control is even more important when no cleaning is performed. These unforeseen facts are reflected by a small number of companies that have adopted "no-clean" techniques and are reverting to cleaning as practical field experience is acquired. Production contamination testing is therefore important, using ionic determination before the soldering process and a new type of ultra-rapid SIR process after it.

INTRODUCTION

Up to recently, little thought has been applied to the reliability problems engendered by the presence of contamination on electronics assemblies or its corollary, cleaning [References 1, 2]. Two military specifications [References 3, 4] pioneered the notion of checking for certain contaminant species in the USA and the UK, but little research has been done to correlate the causes and the effects on the reliability of the finished products, or even to determine the acceptable quantities of residual contamination under any given set of conditions. An important research project has been started by the Swiss Federal Institute of Technology, Zurich to examine the overall aspects of Reliability and SM Technology, under the authority of Professor A. Birolini, Chair of Reliability [Reference 5]. Cleaning is one part of this project, in which a provisional working matrix is currently in the course of elaboration. This will involve at least:

- solder pastes with at least four different chemistries
- reflow and wave soldering
- "no-clean" and five different cleaning techniques
- layout design factors.

The output parameters are, for the moment, less well defined but will probably include:

- Ionic Contamination Testing
- SIR testing under steady 35–40°C/95% RH conditions
- SIR testing under steady 85°C/85% RH conditions
- Vesication testing with a single thin conformal coating
- SIR testing under different test and bias voltage conditions.

It is not envisaged that dynamic electronic functional reliability be determined at this stage as a function of the soldering/cleaning conditions. This is because funding is limited and the cost of determining whether each failure under dynamic conditions is a function of soldering/cleaning or because of extrinsic factors would become astronomical. Nevertheless, if funds to do this became available, the project could be expanded. This

would then become the first academic work that could correlate contamination and surface insulation resistance values to different failure mechanisms. It is without doubt that this would have an enormous practical importance as it is almost universally agreed that, whereas we have an empirical idea of acceptable contamination levels for given applications, we do not *know* what scientifically-proven correlations exist between contamination types and levels and failure mechanisms and, hence, reliability. We therefore base much of our decision-making in this field on conjecture. Unfortunately, such funding could not come from academia and industry has not been able to be too generous over the past year or two, despite the fact that they are the most likely to benefit from such research.

The situation regarding the correlation of cleaning and reliability has recently changed because of two important factors. The first is the discovery that the habitual cleaning solvents, based on CFC-113 and 1,1,1-trichloroethane, were partially responsible for stratospheric ozone depletion. The other is the widespread introduction of surface mount techniques which are somewhat contradictory to good surface cleanliness, hence reliability.

THE MONTREAL PROTOCOL

The Montreal Protocol is an international agreement limiting, and finally forbidding, the use of most ozone depleting substances. It was signed in September 1987 and the first amendment was signed in June 1990. A second amendment will be signed in October 1991. The 1990 amendment was deliberately severe as research since 1987 had shown that the initial measures were insufficient to preserve the stratospheric ozone in quantities ample enough to prevent excessive solar radiation from reaching the biosphere. As the situation has now been shown to be even worse than was thought then, it is no secret that the 1991 amendment will probably be even more severe, to the extent that world industry will be hard put to conform to the probable measures. Early indications (late September 1991) show that the Antarctic "ozone-hole" is starting to be measurable at least one to two weeks earlier than has been possible in past years, but this may also be partially due to more sophisticated instrumentation. A recent news report [Reference 6] indicates a possibility that inhabitants of Tierra del Fuego

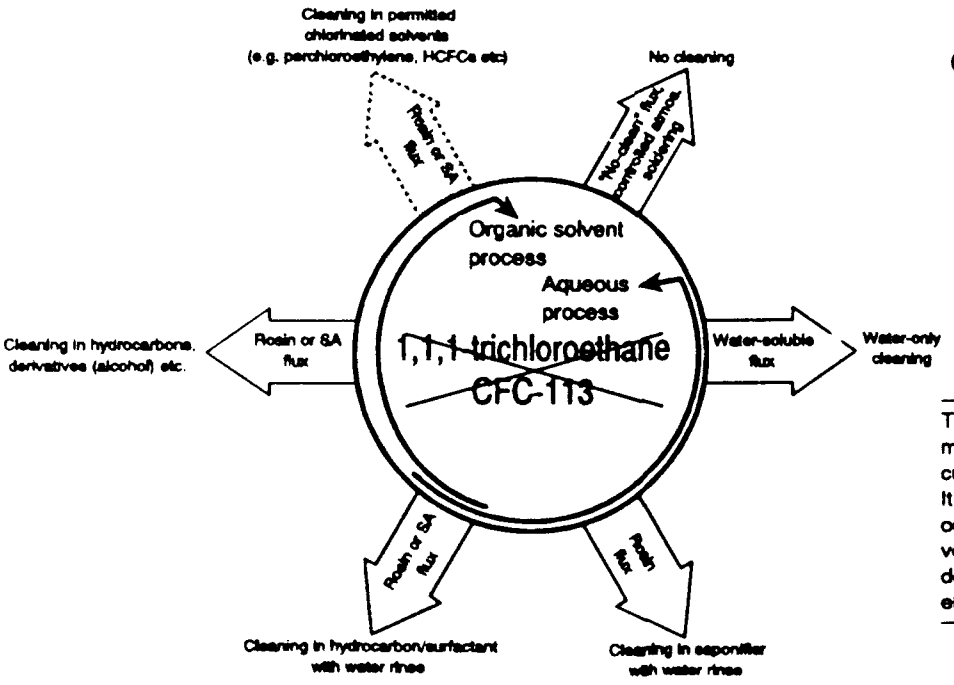


FIGURE 1. Substitutes for Ozone-Depleting Solvents

This diagram shows the main substitutes that are currently being proposed. It is unlikely that HCFCs or other halogenated solvents will take a preponderant position for electronics cleaning.

and Southern Patagonia are suffering from an increase of ultra-violet light-related ocular diseases, ascribed to ozone depletion.

The cleaning solvents most affected by the Protocol are 1,1,2-trichloro-1,2,2-trifluoroethane (CFC-113) and 1,1,1-trichloroethane (also known as methyl chloroform). Both of these are used, amongst other applications, for removing flux residues from soldered printed circuit boards. They are generally sold under a number of trade names. In Switzerland, Germany and some other "head-start" countries, legislation has been passed that will forbid their use as early as the end of 1992 (Sweden since 1 January 1991). It is very unlikely that any derogations will be allowed for defluxing assemblies.

This situation has forced industry to seek rapidly other means of cleaning electronics assemblies or even to abandon cleaning [References 7, 8]. The implications of this sudden change in techniques, in terms of assembly reliability, are not fully known, but neither is a truly dependable yardstick against which to measure the effects of these sudden changes of thought.

Six substitution methods (Figure 1) are commonly being applied to move away from the traditional rosin flux soldering and CFC-113 azeotrope or 1,1,1-trichloroethane cleaning. It is almost indisputable to say that this is causing a revolution in the industry. The traditional method has been "comfortable" because any errors in the cleaning process did not necessarily produce catastrophically poor results and many users firmly believed in the "slosh it around in a bucket of solvent and it was clean" approach. Many users did no contamination testing because of this. Quite apart from the poor science in this approach, it engendered a false sense of security (Figure 2). The first winds of change blew with the publication of the UK DEF-STAN 00-10/3 in 1986 which encouraged the use of aqueous methods, whilst not forbidding the use of halocarbon solvents. This standard was the result of several years' R&D work by the Ministry of Defence who showed unequivocally that the use of many water-soluble fluxes did not produce any deleterious effects on the reliability of the assemblies. At the same time, this standard introduced a more scientifically established test referee method of ionic contamination determination than the MIL method which had pioneered the way more than a decade earlier. This new method was compatible with some of the commercially-available test equipment offered on the market. Furthermore, the International Electrotechnical Commission Technical Committee 52 (IEC TC52) are elaborating a new standard which takes the UK DEF-STAN as its starting point. It is expected that, in time, this standard will be

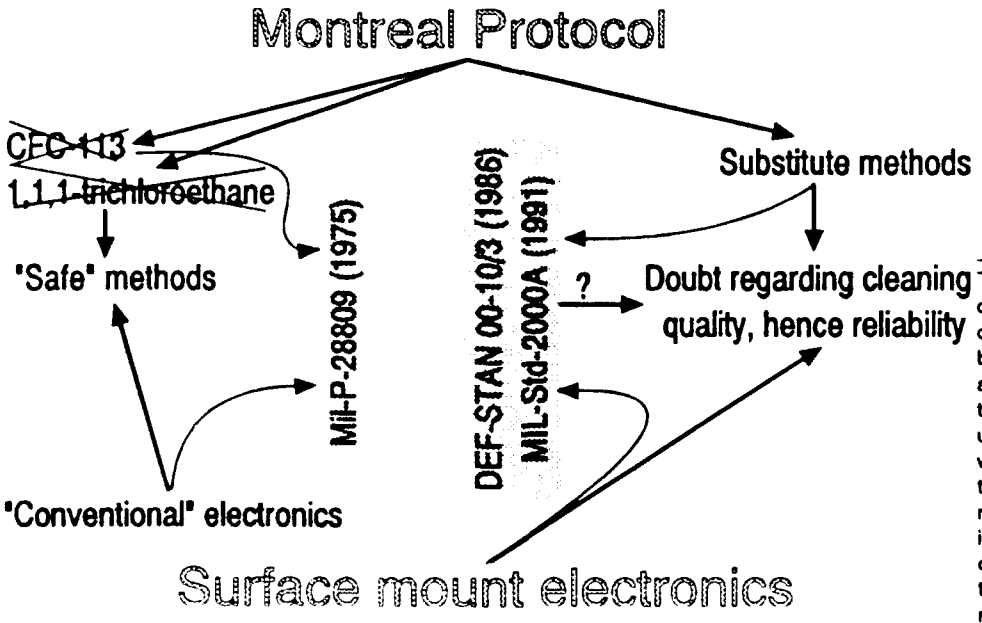


FIGURE 2. Evolution Engendering Doubt

The change from traditional methods of cleaning and assembly leaves a certain amount of doubt as to the quantities of residual contamination that will be left and as to their effect. This means that increasingly scientific methods of contamination testing are becoming necessary.

TABLE 1. Detectability of Contaminant Species

Contaminant	Ionic contamination testing	Surface Insulation Resistance testing
Salt (ionophoric)	Measurable	Effect measurable
Lead chloride (ionogenic)	Measurable	Not measurable
Sugar	Not measurable	Effect measurable
Pure rosin	Not measurable	Not measurable: may improve SIR
Activated rosin flux	Effect measurable	Effect may be measurable
Low-solids rosin flux residues	Effect measurable but not meaningful	Effect may be measurable
W/S flux vehicule	Not measurable	Effect measurable
W/S flux activators	Measurable	Effect measurable
Soluble cutting oils (dried)	Measurable	Probably not measurable
Silicone oil	Not measurable	Not measurable: may improve SIR
Poorly cured resins	Measurable	Probably not measurable
Under-SMD contamination	Measurable	Effect measurable

incorporated in most of the national standards, such as ANSI, DIN, BSS, NF etc., as the signatory nations will have every interest in doing so.

THE EFFECT OF SURFACE MOUNTING

Surface Mount Techniques (SMT) introduced some new parameters into the reliability equation. Some of these, such as the differential expansions of components and substrates, have been the subject of much literature. Defluxing has been another such controversial subject. Its corollary, contamination testing, has been the subject of considerable advances in commercial instrumentation but these could hardly be described as controversial (other than commercial arguments, of course!).

METHODS OF CONTAMINATION TESTING

There are several direct and indirect ways of contamination testing. It is emphasised that no single method can give a complete picture of the situation. All the methods are therefore complementary to each other, with little overlap. The two commonest tests are ionic contamination testing (ICT) and surface insulation resistance (SIR) testing. Table 1 shows that there is not necessarily any correlation between the two. However, if a single ionic contaminant species is studied, a correlation may be found. This has no practical value as real contamination is never just a single type. In the case of similar groups of species, such as cleaning post-soldering rosin flux residues, a weak correlation may be found across a few flux types of a single family and a few solvent types of a single family, but even this disappears immediately on comparing one flux type cleaned using radically different methods or two distinct flux types cleaned by one method. There is a danger in that if SIR values and ICT values are plotted on a log-log graph, it may appear that a weak correlation exists when this is not the case. Only mathematical analyses of variance (ANOVA) give reliable indications of whether there is a "fit" between two sets of figures and its reliability.

The following list gives, in an approximately decreasing order of typical importance, the most usual methods of contamination or cleanliness testing and related controls.

- Ionic Contamination Testing
- Surface Insulation Resistance Testing
- Vesication ("Pressure-cooker") Testing
- IPC "Acetonitrile" Testing (2 methods)
- Ionic Chromatographic Testing
- Light Diffusion Testing
- Atomic Evaporation Testing
- "Wet" Analyses
- Visual inspection.

Some of these are production tests, some are qualification procedures but many of them are useful in both cases. It is proposed to discuss the more important ones in detail.

IONIC CONTAMINATION TESTING

Ionic contamination testing is often described as the workhorse method for both production testing and as a qualification procedure. Briefly, it consists of immersing the assembly or the component to be tested in an ultra-pure solution of isopropanol in water. Any ionic contaminants amongst the contamination washed off will cause the solution conductivity to rise. This change of conductivity can be interpreted mathematically as an equivalent weight of sodium chloride (i.e. the weight of sodium chloride that would have had an identical quantitative electrical effect, had the contamination been only pure salt). For convenience, this is usually related to the surface area of the assembly or de ice. As yet, no standard units have been generally adopted but in Europe and Asia the preferred expression is $\mu g.cm^{-2}$ eq. NaCl, rarely mg/dm^2. In North America, both metric and imperial/metric mixtures are common, e.g. µg/sq.in.

There are a number of commercial instruments available for doing these tests, from North America and Europe. These vary widely in sophistication from simple, low-cost, manual testers to very complex computerised types. The former are not very accurate (by their principle) and are very labour-intensive, so are useful as an indication for occasional informative testing only. Where regular testing is imposed or where a better precision is required, at least a microprocessor controlled instrument is necessary, preferably a computerised one.

Users of these instruments have expressed consternation (and rightly so) that similarly contaminated assemblies tested in different instruments give different results, sometimes in a ratio of 2:1 or even more. As sophistication rises, so these differentials are diminishing. The reasons for these inaccuracies are various: poor temperature compensation, different agitation resulting in different dissolution of contaminants, ill-defined starting conductivities, different tank designs creating variations in extrinsic ion absorption from the air or the constructional materials, errors in measuring low values of conductivity, errors in the method of making up the test solution, different area:volume ratios and so on. An initial attempt was made to define "equivalence factors" in 1978, to correlate a few instruments to a common denominator. This was unfortunate as many persons followed the results of this attempt too literally, even though the tests were carried out with a single, raw unused flux. The residues bore no resemblance to what was found on cleaned boards after soldering. Furthermore, many persons considered that the "equivalence factor" held good for completely different models of testers which bore the same name, even though they patently operated under widely different conditions.

The European Space Agency commissioned a study in the early 1980s for the Ariane project. This showed very clearly that "equivalence factors" were virtually meaningless, as the values could vary widely with one instrument under practical conditions. Simply a change of flux or soldering parameters could change the factor by a multiplier of two or more. This study showed that instrument errors were not always negligible. As a result, the ESA chose a computerised European model as being the most precise.

Of course, the American military authorities have been aware that the specifications based on the MIL-P-28809 (1975) referee method are far from perfect with many undefined parameters. Until recently, the usual cleaning method of a CFC-113 azeotrope to remove MIL-F-14256 type fluxes was so "fail-safe" that little priority was given to correcting the anomalies in the specification. The advent of Surface Mounting and alternative fluxes and cleaning techniques are changing this and an IPC/EMPF study is under way to remove

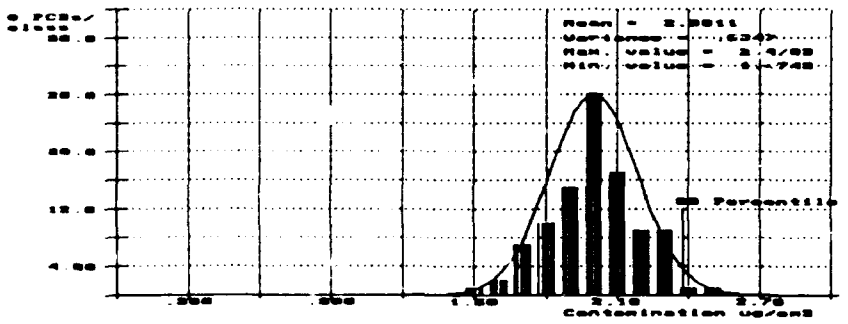


FIGURE 3.
Histogram Showing
Excessive
Contamination

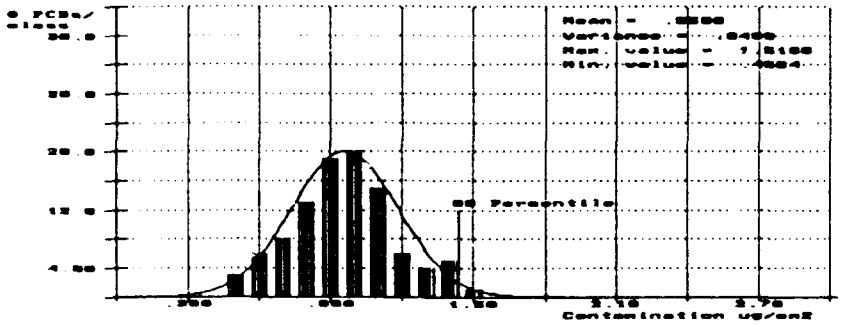


FIGURE 4.
Histogram Showing
Unnecessary
Cleaning

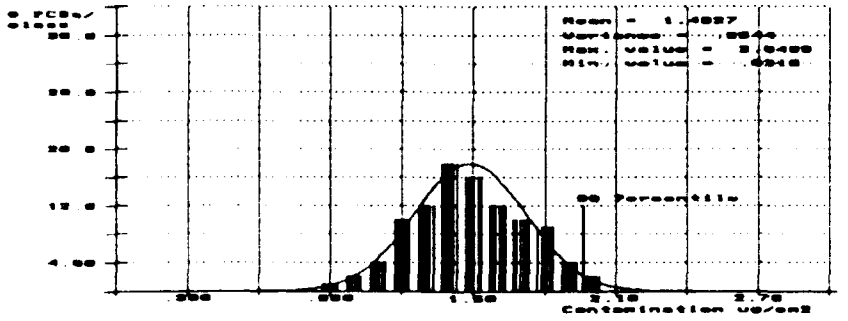


FIGURE 5.
Histogram Showing
Poor Process
Control

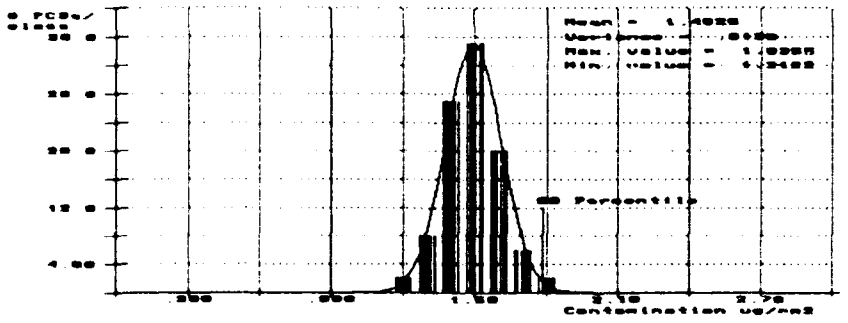


FIGURE 6.
Histogram
Showing Tight
Process Control.

some of these anomalies. To give an indication of the extent of these anomalies, a theoretical worst-case calculation of the MIL-P-28809 referee method reveals that the limit value should be situated at 1.3 $\mu g.cm^{-2}$ eq. NaCl. Practical interpretations, using instruments as well as the referee method, have varied from between 1.55 and 3.2 $\mu g.cm^{-2}$ eq. NaCl. According to other authorities, such as the UK Ministry of Defence, a real contamination level of 1.50 $\mu g.cm^{-2}$ eq. NaCl is the limit which is acceptable, as measured with a commercial instrument or their referee method. This figure was derived after years of laboratory and practical trials. This implies that the reliability of some MIL-spec related electronics may be marginal. In fact, informal discussions with the MoD reveal they are considering tightening their specification to 1.00 $\mu g.cm^{-2}$ eq. NaCl for Surface Mount Assemblies, *related to the pasted area only and not to the full PCB area*. This will imply a typical 5–10 times more severe specification than has hitherto been current on either side of the Atlantic.

If only to eliminate this "fuzzy" lack of precision, it is this author's opinion that the forthcoming IEC specification can be useful. It will not specify limit values but individual authorities will at least have a yardstick common to all. As a simple suggestion, the following values may be indicative of real life, as it is now:

Implanted medical electronics	0.3 $\mu g.cm^{-2}$ eq. NaCl
Military, avionics SMD	1.0 $\mu g.cm^{-2}$ eq. NaCl
Car engine and brakes SMD	1.0 $\mu g.cm^{-2}$ eq. NaCl
Other military, avionics, car	1.5 $\mu g.cm^{-2}$ eq. NaCl
Industrial, telecoms, computer	2.0 $\mu g.cm^{-2}$ eq. NaCl
Other professional	2.5 $\mu g.cm^{-2}$ eq. NaCl

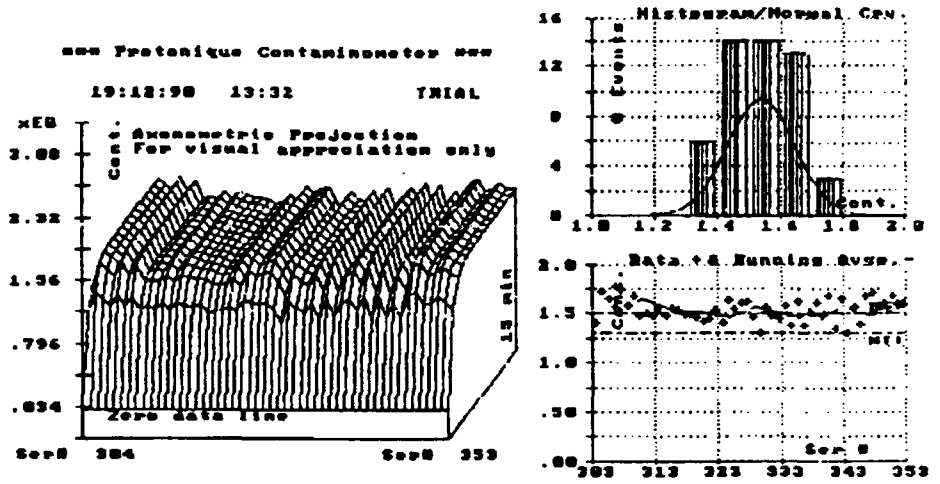
Obviously, these suggestions may be modulated according to the real requirements. For example, if a particular telecommunications device has large conductor spacings, is used only on low voltages in an air-conditioned room, then the value can probably be upped to 3 $\mu g.cm^{-2}$ eq. NaCl or more (indeed, it may be that cleaning can be dispensed with altogether and the circuit can be soldered with a "no-clean" flux). On the other hand, a street-housing multiplexer with fine circuitry and high-impedance operation must work reliably as servicing costs would be prohibitively high, so that the limit value should be reduced to 1.5 or even 1 $\mu g.cm^{-2}$ eq. NaCl.

In real life, no process is ever perfect. This applies equally to assembly/soldering/cleaning. This means that there will always be residual and measurable contamination. The end value will be a function of, perhaps, a dozen or more parameters, each with its own tolerance. The slightest variation in any of them, such as flux density, power voltage feeding the fusing oven or cleaning temperature, will alter the residual ionic contamination. This means that they will all contribute to a tolerance of the end value. The question must therefore be asked as to what must be specified on deciding a limit. Various ideas spring to the mind, such as:

- absolute limit value
- mean limit value
- 99 percentile limit value.

Let us look at what these mean. Up to now, most specifications lay down such an absolute limit value, no matter how they are interpreted. For argument's sake, let us suppose that the limit value is 1.5 $\mu g.cm^{-2}$ eq. NaCl. A batch of 100 circuits, representing, say, 30 minutes production, is sampled and one PC assembly is tested. It reveals an ionic contamination of 1.47 $\mu g.cm^{-2}$ eq. NaCl, therefore the batch passes. But the histogram of the contamination on the 100 boards is as shown in Figure 3 (these histograms are not real cases but are mathematically modelled using probability techniques: they therefore are indicative of typical cases that could occur in real life). This shows that, as luck would have it, many of the other boards are not only outside the limit, they are dangerously so: the selected board just happened to hit that 99:1 chance of being the cleanest one. Of course, exactly the opposite can happen: you hit on the dirtiest one at, say, 1.52 $\mu g.cm^{-2}$ eq. NaCl, so you clean the lot again (Figure 4). However, this costs you an arm and a leg when 99 boards were already within specification. Any statistician can say that a single absolute value can be valid only if every single circuit is individually tested.

A mean value is equally meaningless, or even more so. Still keeping the same hypothetical limit of 1.5 $\mu g.cm^{-2}$ eq. NaCl, this time as a mean, the two curves in Figures 5 and 6 both display a mean of slightly



*** Protonique Contaminometer ***

Statistical analysis of a Contaminometer file:
File name: \DATAFILE\sample.DTA

The file being analysed relates to following data:

Circuit #	1st used	Ser #	# items	Area cm2	Vol cm3
TRIAL	02:10:87	353	50	188.71	.00

Date and time of analysis: 19:12:90 13:35

Raw data of file extrapolated to 15 mins, starting at last test:

1.5933	1.6119	1.6759	1.6865	1.5812	1.7125
1.6838	1.3910	1.5693	1.3861	1.6513	1.3446
1.6738	1.4830	1.6128	1.5225	1.3786	1.6248
1.3848	1.5886	1.4499	1.4786	1.5664	1.3873
1.4695	1.6239	1.6856	1.5565	1.6347	1.4858
1.5325	1.4477	1.4254	1.4682	1.4930	1.4994
1.5368	1.5542	1.4819	1.5624	1.4798	1.5856
1.4763	1.6865	1.5811	1.7302	1.5690	1.6537
1.7161	1.4889				

Mean	Standard deviation	Variance
1.5377	.1071	.0115

Percentile probability of measures meeting theoretical MTL-P-28809 limit:
1.33
Percentile probability of measures meeting DEF.STAN 00-10/3 limit:
36.25
99% of the tests will have a contamination of less than
1.79 ug/cm2 eq. NaCl

Least squares fit shows progression is slightly increasing
Regression analysis of variance shows reliability of least squares fit to be not necessarily good (alternative hypothesis of H1 > 0.1).

Histogram data. X: classes from ... values Class interval
Y: number of events in each class. Specific deviation

X	1.00	1.10	1.20	1.30	1.40	1.50	1.60	1.70	1.80	1.90	.10
Y	.	.	.	6.	14.	14.	13.	3.	.	.	6.97
Y%	.00	.00	.00	12.00	28.00	28.00	26.00	6.00	.00	.00	

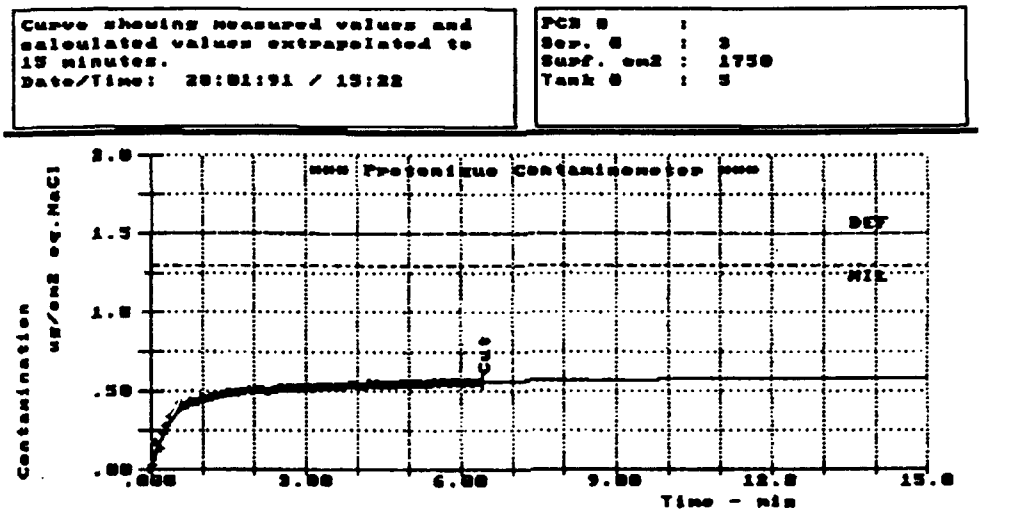
FIGURE 7. Reduction of Statistics with Probabilities

under the limit, but one shows a very tightly maintained process with a narrow "bell". The other has a wide "bell", indicating the possibility of major deviations from the norm. Even worse, the curve may be skewed, so that deviations of three or four times the mean would be possible. This is therefore not a valid solution, either.

The third possibility is to place the limit at the 99 percentile, as shown in Figure 4. This means that 99% of the integrated area of the curve must be below the limit value. Initially, when putting a process into service, the absolute limit value must be used and the risk taken that the first of the above problems occurs. This risk may be minimised by a) initially measuring two circuits per batch, instead of one and b) measuring even more if either come to within 95% of the limit value. Once, say, 30 or 50 circuits have been tested with zero failures (even if some are close to the borderline), the distribution can be analysed to determine the *probability* of a board not meeting the specified limit. Hopefully, this will be a fractile approaching unity or a percentile close to 100, say 0.998 or 99.8 respectively (they both mean the same thing). Thereafter, as long as the measured values are well under the limit, it will be sufficient to calculate the percentile probability occasionally, say, after every ten or twenty tests. If it starts to drop, then the warning bells start to ring. If any single test is over the limit or even approaches it closely, then the probability must be immediately recalculated and, as long as the percentile probability remains over 99, then all is well: it probably means that the "maverick" just happened to exceed the limit by an unlucky chance. Once the probability drops to 99.0, then action must be taken. If it shows that the percentile probability of meeting the specification is between 99.0 and 99.1, the safety margin is small and more frequent calculations will be required. This procedure seems complicated, but it takes luck out of the equation and some commercially available contamination testers are able to do the calculation automatically on the last 50 tests in a file. Above all, except for the start-up period after a process change, probability is a mathematically calculable parameter and cheating is almost impossible with well-designed software: if a single test seems abnormally high, the indication is almost immediate whether something has gone wrong or whether the value is acceptable. In other words, it is statistically valid which none of the other methods are. In the case shown, the percentile probability of a test being lower than 1.50 $\mu g.cm^{-2}$ eq. NaCl is as high as about 99.6 and the chance of any one test reaching the value shown of 1.5166 is about 1 in 500. The 99 percentile probability level is about 1.45, which is under the arbitrary limit value fixed at 1.50 $\mu g.cm^{-2}$ eq. NaCl. If further information is required, an analysis of variance will permit a hypothesis to be calculated indicating the reliability of the interpretation to a normal distribution curve, although this is evident to the eye by comparing the shape of the histogram to that of the curve. In all four figures, the hypotheses are very good.

It may be argued that not all testers can do the statistical analysis (Figure 7). Albeit laborious, those that cannot can have the results calculated manually. If this is too difficult, there remains the absolute limit value. This means that if a specification quotes a 99 percentile limit of, say, 1.5 $\mu g.cm^{-2}$ eq. NaCl, those who are equipped to use it as such can profit from it. Those who have an older instrument without the automatic software can still use 1.5 $\mu g.cm^{-2}$ eq. NaCl as an absolute limit value. This interpretation is "fail-safe" in that they are no worse off than today and that no test exceeding the value would be acceptable. *This author strongly recommends that any company or authority laying down new specification limits adopt a 99 percentile limit with the proviso that an absolute limit of the same value would be equally acceptable should the equipment used not permit easy calculation of the probability.*

Another problem which has become accentuated by the Montreal Protocol is that of ensuring that contamination trapped under SM components be measured. If the choice falls on a more ionic flux or cleaning method than the traditional RMA or RA/CFC-113 combination, it is important that the cleaning be even more effective under the components. That being so, it is equally important that any residual contamination there be measurable. Two techniques have been employed to improve the measurements. The first is to heat the solution and to increase the agitation by a more vigorous circulation. This is a low-cost, simple system but not entirely effective as rosin flux residues under a large component close to the board will still not be removed in a reasonable time. Furthermore, heating the solution increases the fire risk, especially with a 75% isopropanol solution, and increases the evaporation of alcohol, necessitating more maintenance. The under-components contamination is added to that of the general surface contamination and averaged over the whole surface. There is no way of knowing the contamination levels under the components. The other way presupposes that it is impossible to remove all the contaminants under the components. The contamination is extracted with a vigourous but non-turbulent flow, for up to a maximum of 15 minutes, even though it is not all removed. The



*** Protonique Contaminometer ***

Result of Contaminometer test:

Date and time of test	: 28:01:91 / 15:25
File name/circuit number	: \DATAFILE\tank5.DTA /
Length of true measurements (mins/secs)	: 6 / 24
Value at out (ug/cm2 eq. NaCl)	: .56
Value at 15 mins (ug/cm2 eq. NaCl)	: .58
Value at asymptote (ug/cm2 eq. NaCl)	: .58
Percentile figure of merit for fit	: 99.70
MIL-P-28809 (theoretical worst-case)	: meets.
DEF. STAN. 00-10/3	: meets.

Two distinct contamination sources detectable.

Arbitrary commentary on results:

Contaminations detected:
   Contamination type # 1
Asymptotic value (ug/cm2 eq. NaCl) : .44
Very fast dissolving (mineral salts, acids, bases etc.).
   Contamination type # 2
Asymptotic value (ug/cm2 eq. NaCl) : .14
Very slow dissolving (old rosin or old fingerprints etc.).

Relative danger of COMBINATION of level and type of contamination:
Very low!

Test precision is high!

The above commentary is derived from experience for very high-reliability applications but has not been scientifically established. Interpretation should be carefully made. It may be possible to upgrade the comments for lower reliability applications or for work in temperate climates only.

FIGURE 8. Reduction of Print-out Showing Two Contaminants

curve is then subjected to mathematical modelling from which a formula is derived. This formula can then be extrapolated to infinite time to find the asymptotic contamination level, representing the total, as if it had all been dissolved. As a rule, the precision using this technique is reasonably high provided that the contaminants are real ones, as met with in practice. If they are artificially induced ones, the curves may become so bizarre that no models can exist. The real advantage of this process is that analysis of the curves reveals, to within a few percent, the portions of the total asymptotic contamination under the components and on the surface. If it is known that the surface area under the components is, say, 20 percent of the total, then a rapid mental calculation will multiply the stated part of the under-component contamination by 5 to reveal the local value. Comparative tests between assemblies measured by this method and similar assemblies with the components mechanically removed reveal a very close correlation of results, with several different chemistries. Figure 8 gives a reproduction of a sample print-out showing two independent contamination sources.

One of the perennial questions is where ICT fits in with "no-clean" techniques. In reality, there are three different questions. With resin "no-clean" fluxes where the resin is insoluble in the alcohol/water mixture, it may be said that ICT is meaningless, as only surface contaminants on top of the flux residues will be looked at. Equally, rosin or soluble resin flux residues will also be somewhat meaningless or, at least, difficult to interpret as the measurement will include the activators that are normally held harmlessly in the resin/rosin matrix: this is the other extreme. On the other hand, soldering using a matrix-less flux, such as is often used for controlled atmosphere soldering, or with a carboxylic acid mist in the soldering zone will be meaningful, as the residues measured will be the real contamination that would have harmful effects on the reliability of the board. Tests of previously cleaned boards coming out of a controlled atmosphere wave soldering machine have revealed typical ionic contamination levels between 2 and 6 $\mu g.cm^{-2}$ eq. NaCl. This value would generally be considered as incompatible with high-reliability electronics. As a parentheses, it must be mentioned that cleaning after controlled atmosphere soldering is, comparatively speaking, child's play.

Where an excellent reliability is required, within the limits of any specific "no-clean" flux of the resin/rosin matrix type, the best results may be assured by checking the cleanliness *before* soldering. If the PCB or the components have a strong dose of contamination prior to fluxing, the solvents in the flux may dissolve it. This means that the physical quantity of contamination plus activators will probably exceed the capacity of the resin or rosin to encapsulate it in a safe matrix. The result will be catastrophic under humid conditions. Checking that the ionic contamination is close to zero before fluxing is a good insurance policy to prevent such a mishap. At the same time, there will be little risk of the flux action being perturbed by the presence of extraneous contaminants.

Another disputed matter is the proportion of isopropanol there should be in the test solution. The first tests were manual sprays with very short integration times and specifically designed uniquely for testing rosin flux residues. Understandably, a high percentage (75%) of IPA was chosen to dissolve the rosin faster. With modern immersion techniques, time is less important as the integration can continue until the curve levels off. Also, rosin appears less frequently amongst the residues. For these reasons, the UK DEF-STAN 00-10/3 selects 50% with numerous advantages:

- Sensitivity better by a factor of two
- Solution much less flammable
- Solution much less volatile—less maintenance and less risk of operator overexposure
- Specific heat of solution higher, creating more stable temperature conditions
- Risk of saturation of metallic salts reduced by a factor of two

Of course, this is a compromise and to weigh against these advantages are the following disadvantages:

- Poorer solubilisation of rosin
- Surface tension of solution about 17% higher
- Viscosity of solution about 21% higher.

The forthcoming IEC standards will not specify a single percentage but simply offer the choice between 0, 50 or 75 percent IPA (the 0% IPA solution is specifically for PCB manufacturing applications, after electroplating, where the added sensitivity will be much appreciated). In practice, the ease of use of 50% solutions is an

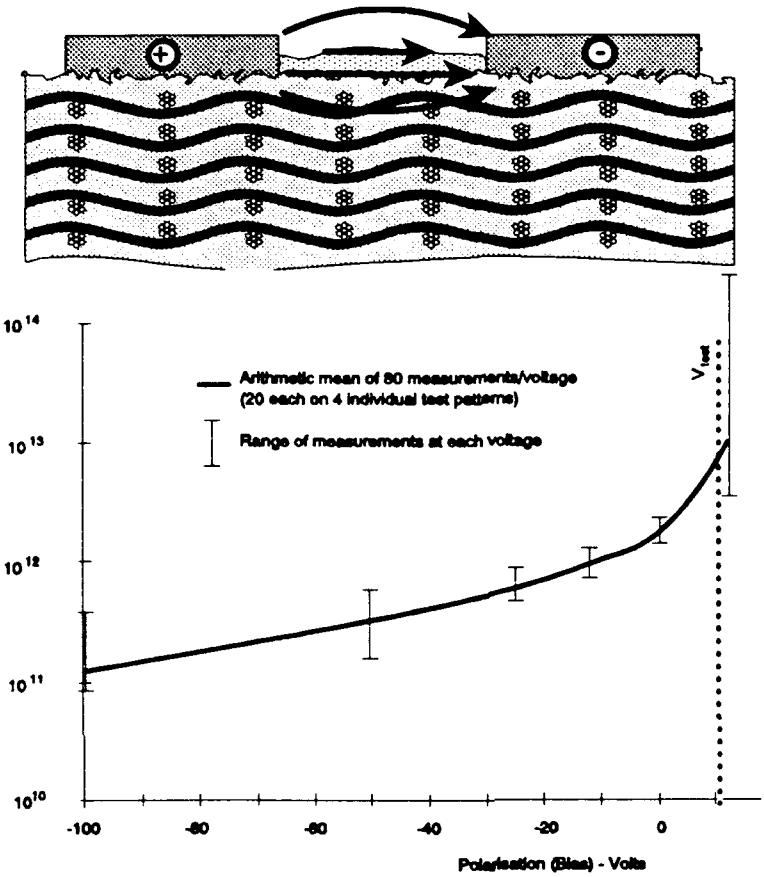


FIGURE 9. Four Leakage Paths between Conductors

FIGURE 10. Variation of Apparent SIR with Bias Voltage

It is evident that the maximum precision is obtained without a bias voltage. Positive voltages give the least precision, but the highest apparent reading. Note that with negative bias, the instrument precision is in the highest range.

added feature. Of course, for a given level of contamination, both solution percentages give essentially similar results with usual flux residues although the time taken to reach this level may be longer.

Perhaps another important point is checking the calibration of ionic contamination testers. This is a very tricky operation. Some of the more sophisticated models do an automatic calibration check each time they are switched on.

SURFACE INSULATION RESISTANCE TESTING

SIR testing is much more controversial than ICT. This is because there are a multitude of standards contradicting one another and most of these date from work done 25 or more years ago, so do not reflect modern packaging technology. At that time, most available instruments worked at least at 100 V and printed circuits had typical conductor spacings of 0.5—1.0 mm. The voltage gradients were therefore typically 100—200 $V.mm^{-1}$. Today's PCB has conductor spacings of 0.075—0.150 mm. To maintain the same voltage gradient, it therefore becomes essential to reduce the test voltage by an order of magnitude. With modern technology, this has become feasible. It is aberrant to use the old voltages with the new spacings: put 100 V across the finest of the IPC-B-25 test patterns and you have a voltage gradient which exceeds established standards by a factor of nearly 4. In addition, nobody really knows what SIR testing means. If you apply a voltage between two conductors on a PCB (Figure 9) and a current flows, is this through the humid air, along the contamination on the surface, along the tortuous surface profile or through the epoxy resin (possible via the glass fibres with their silane treatment)? Undoubtedly, it may be a combination of any two or more of these, probably, the most often, all four [Reference 9]. How can one make sense of this, then? Absolute sense, probably never. Relative sense may be more possible.

The first thing to do is to analyse what we want SIR to do. We do not want to have errors due to air conduction [References 10, 11]. It is surmised that much air conduction under humid conditions is ionic due to water molecules orienting themselves in the electric field generated by the bias or polarisation voltage. As opposed charges on adjacent molecules will then face each other, there will be a mutual attraction and molecular clumping occurs. This, in turn, forms a water aerosol with each particle charged. There will thus be a distinct tendency for the water to be attracted to the conductors where it will wet them. As this area will become low in humidity, more will fill it and this will form a continuous process. This hypothesis explains the non-linearity of air conduction which has been observed. Water deposits on the board will, of course, also give misleading results. These errors can be mitigated by ensuring that the voltage gradient should always be as low as possible, certainly less than 20 $V.mm^{-1}$, implying no bias and low measuring voltages.

We are also not interested in currents through the epoxy resin. Epoxy is far from an ideal electrical resin as it inevitably contains ionophores, usually sodium chloride [Reference 9]. It is the presence of these molecules, albeit in small quantities in electrical grades, that explains the high dielectric constant, the high hygroscopicity, the high power factor and the poor high-frequency characteristics of the polymers. If these ionophores are subjected to a high electric field, they ionise and the sodium and chloride ions tend to migrate in opposing directions. As a rule, the radius of migration is so small that, when the field disappears, they will recombine, but the average time required for this is of the order of minutes or hours as the energy levels are extremely small. The ionic flow, on the other hand, is comparatively rapid when the field is applied and the energy for this is supplied by the applied voltage. The current flow is therefore not only in relation to the applied voltage, it is also in relation to the degree of ionisation of the ionophores at any moment. Reversing the field therefore causes exaggerated current flows which, with high voltage gradients in both directions, may take hours to stabilise. This phenomenon is made very visible by the apparent SIR, measured at low voltages under dry conditions (so that the presence of water molecules does not create any false readings), within one minute after ceasing the application of a bias voltage (Figure 10). The conclusion to be drawn is that the most precise readings of the true SIR can only be made at low voltage gradients with no bias voltage of either polarity, with the test voltage applied for a minimal length of time necessary to make the measurement. It should be noted that the presence of humidity changes the values but not the principle of this phenomenon.

This leaves the true SIR and that due to the presence of surface, absorbed or adsorbed contaminants. In view of the tortuous path left on an epoxy substrate surface after etching the copper, if the surface is correctly polymerised and no contaminants are present, the true SIR will be extremely high. The rest of the measured readings will therefore be due to the presence of contaminants, which is what we are after measuring, in any case.

The above precisions all mention low test voltages and no bias: is this sufficient for measuring the effects of above-surface, adsorbed and absorbed contaminants? Under the best conditions, dry and at room temperature, the results are measurable but the precision may be doubtful, even with a double-comb pattern with more than 2,000 squares. At 35°C and 95% RH, suitable low-impedance ballistic instruments operating at about 10 V will measure and analyse automatically the effects over any period of time. Such instruments do allow the application of bias voltages, even though they reduce the precision. Because the measuring circuit itself is of very low impedance, extensive Faraday cage shielding is not necessary, nor are triboelectric effects along the wires important. On the other hand, the effect of the losses in the polytetrafluoroethylene-insulated connecting wires, which are not even shielded, is compensated for in the instrument calibration, which means that the length is fixed, to a tolerance of about ±100 mm (4").

The same type of instrument can be used for other than traditional qualification procedures or laboratory test lasting up to, say, 56 days. As it is computer-controlled, another software possibility is to place samples (up to 96) of the day's production in a special chamber and bring the temperature up to 90°C at low humidity. The chamber is then humidified and kept at 85°C 85% RH overnight. Low voltage tests are carried out with no polarisation bias, each test point being measured every 15 minutes for 8—10 hours. The important point here is not the absolute values of SIR (although this is interesting), so much as the changes from the moment that the humidity enters the chamber. Properly interpreted by the computer, these changes can give a valuable indication of the nature of any contaminants and the likelihood of future troubles. Some of the test patterns can be placed

under critical components. It is emphasised that this is a relatively rapid, non-destructive test. When the operator arrives at work, the computer print-out will be waiting for him and he can either release the circuits cleaned the previous day or rework them, according to the results. Another important point is that such an instrument should be able to analyse groups of circuits. If the day's production includes 1,000 circuits of Circuit A, 500 of Circuit B and 1,200 of Circuit C, the 20 samples of A, the 10 samples of B and the 24 samples of C should each have individual group statistical analyses as, in all probability, there will be widely varying conditions under the components. If all the 54 circuits were grouped together, the analysis could become impossible but, even if it was not, it would be almost meaningless and certainly misleading.

This type of measurement will be especially interesting for circuits soldered using a flux which is not subsequently removed. In reality, it is the only valid *production* test under these conditions.

VESICATION TESTING ("PRESSURE-COOKER TEST")

This is a simple method [References 12, 13] for determining the proneness to vesication, some forms of which are also known as "mealing". The test is usually considered as destructive, although is not necessarily so with high-quality components. The recommended way to proceed is to take a board after cleaning and drying and dip it very slowly into a 1:1 diluted monocomponent polyurethane conformal coating lacquer. Extract it again vertically very slowly so as to obtain minimum thickness of coating. Allow it to cure thoroughly. The board is then placed in steam in an autoclave running at about 120°C for 48 hours or so. If an autoclave is not available, a domestic pressure cooker may also be used, but care must be taken not to allow it to boil dry. Visual examination detecting non-adhesion of the coating, the formation of blisters or vesicles or the formation of a milky appearance which, under strong magnification, consists of myriad microscopic vesicles, will be an indication of the presence of vesicating contaminants. If they exist, these may be either ionic or non-ionic but will be somewhat hygroscopic. A single hair, cotton or paper fibre will often trigger vesication along itself, so that the hygroscopicity can be of a lower order than produced by salt or other deliquescent materials.

IPC "ACETONITRILE" TESTS

Acetonitrile is a banal synonym for methyl cyanide. The latter term is to be preferred as it gives a better image of the volatile and highly toxic substance it is. Of common, relatively low-cost, solvents available, it has two attractive properties: it is easily obtainable in very pure qualities and it dissolves a wide spectrum of contaminants. Basically, the test [Reference 14] consists of applying a few drops of the substance *under a good fume hood* to a part of the circuit where contaminants are suspected to exist. It is then transferred, along with the dissolved contaminants, to a clean microscope slide, where the methyl cyanide is allowed to evaporate. Visual examination of the slide will reveal any contamination dissolved from the board. If more information is needed, infra-red spectrography will allow an analysis to be made.

ION CHROMATOGRAPHIC TESTING

This is also an extraction procedure whereby individual ions may be detected and measured. The most practical manner of proceeding is to do a standard auto-integrating ionic contamination test and extract "before" and "after" samples of the solution. They are analysed in an ion chromatograph and the difference represents the ions dissolved from the board. A fully automatic sample extraction and analysis system may be incorporated into certain computerised testers of the "static" type, so that the printer, after a test, will print out the total ionics per unit area as equivalent sodium chloride and then the actual level of some individual ions. A chromatograph for one or two ion species families will be an acceptable price but one which will indicate the levels of copper, tin, lead, sodium and nickel as cations and halides, sulphates and nitrates as anions will be quite expensive.

LIGHT DIFFUSION TESTING

This consists of passing a short wavelength (green) coherent light beam through a solution used as a contamination extraction medium [References 12, 13]. The presence of micellar molecules, likely to cause lowering of SIR, will be detected by sensitive optoelectronics normal to the light beam axis, thereby recording

the amount of optical diffusion. The solution is initially regenerated by reverse osmosis. This test is rarely practised as the equipment cost is high, the sensitivity is only just sufficient and it is specific to very long molecules (more than a quarter wavelength) or to micelle clumps.

ATOMIC EVAPORATION TESTING

If a drop of solvent is placed on a contaminant to which it has an affinity, its evaporation rate will be modified. If the conditions of evaporation are fixed and the quantity of evaporated solvent can be measured, a good measure of the quality of the surface can be obtained. Under the best conditions, this method may be sufficiently sensitive to measure down to monolayers. The solvents used are varied and are modified by exchanging a few of the carbon-12 atoms for carbon-14, which is slightly radioactive. The total radioactivity of the solvents is negligible and there are no restrictions on their sale in the quantities involved. No particular safety precautions are required, different from the handling of standard solvents. A drop is placed at a convenient point and the evaporation is controlled in a nitrogen stream in which a G-M tube detects the presence of the carbon-14. A computer does the rest. The method is used for many different applications, including cure testing of solder masks and conformal coatings, the presence of diverse contaminants etc. The cost of the equipment and the test itself is very reasonable and this could be a useful adjunct to many well-equipped laboratories.

"WET" ANALYSES

It is not very frequent that recourse must be made to analytical chemistry wet techniques to find out the causes of contamination. As a general rule, these are employed for debugging rather than for routine contamination determination: i.e. to try and identify, on failed assemblies, a source of contamination that has caused a problem in service. As the effects of contamination are frequently very local, often associated with single points, recourse is often made to microanalysis. Examples may be to determine which substances have been responsible for a given corrosion at one point on a board or to extract the contents of a vesicle with the finest hypodermic needles.

A well-known wet method is useful for determining if a deposit contains rosin: this is the sugar/sulphuric acid method described in standard literature [References 12, 13]. It can be useful at a large scale, on a filter paper, or as a microanalytic technique, observing the reaction on a glazed ceramic tile through a microscope.

VISUAL INSPECTION

Contamination detection on cleaned circuits is difficult using visual techniques. Occasionally, phenomena may be observed but, if these are visible to the naked eye, they are usually very gross problems. Even microscopic examination is of doubtful utility in most cases.

The main problem is being able to interpret correctly the results. Since users have tended away from CFC-113 cleaning which frequently left a monolayer of rosin over the board, including the metallic surfaces, many have complained that their new method is not as good as it leaves a layer of something on the solder joints. Examination shows that there is no contamination: in fact, the cleaning process has improved and that the hitherto brilliant solder joints are no longer protected by the monolayer and oxidise slightly on contact with the air, giving them a slightly matt appearance. Another common misinterpretation is with so-called "white" residues. There are at least a dozen catalogued causes for this. One of the most frequent ones is that the surface of a silk-screened solder resist is not correctly or, at least, entirely cured. During the cleaning process, the surface is attacked slightly, perhaps removing a few micrometres of resin. The alumina fillers are thereby exposed (they are invisible in the resin as the refractive indices of alumina and resin are nearly identical), giving the appearance of a whitish deposit but which isn't one. Many production engineers can cite cases where visual misapprehensions have occurred. The best advice is to try and keep an open mind to *all* the different possibilities and not jump to the first intuitive conclusion.

The means used for visual examinations can often make enormous differences in the facility for diagnoses, the angle, colour and intensity of the light, for example. Linearly polarised light is sometimes also useful. If fluorescent dyes are incorporated in conformal coatings, ultra-violet "black" light will sometimes silhouette

small surface contaminations that would otherwise be almost invisible or reveal traces of coatings where they, themselves, are undesirable, such as on contacts.

PROCEDURES

There are four basic procedures that are used for contamination control:

- Process qualification
- Production testing
- Debugging
- Process checking.

Each of these is equally important.

PROCESS QUALIFICATION

Process qualification must be done logically, starting with testing incoming PCBs and components for contamination, selecting from as wide a choice of suppliers as possible. It includes evaluating the soldering/cleaning chemicals and processes for the best soldering quality and the best cleanliness (this qualification alone can easily take a man-year by experimental methods, less if you engage a specialised expert). Taguchi optimisation, as offered on the software of some contamination testers, is a useful tool for this [Reference 15]. Long-term reliability is an issue at this stage and SIR tests are almost a *sine qua non*, as are also vesication tests.

Only after passing through all these stages and proven that the process is reasonably constant can it be put into full production.

PRODUCTION TESTING

In many cases, this is confined to ionic contamination testing to an external or internal standard limit level. Whether the limit is realistically set or not must be decided with a view to the service conditions of the electronics. As explained earlier, it is preferable to use 99 percentile limits, where possible.

If "no-clean" fluxes are employed, contamination testing should be done before fluxing to prevent prior contamination from upsetting the residue balance.

ICT frequency is a thorny subject. MIL specs evoke a minimum of 5 tests per working shift. This may be too frequent or not frequent enough. If only twenty high-tech boards are produced per day and are cleaned in a small batch cleaner, it would seem that 2 tests in a manual machine may be sufficient. If 2000 boards are produced in a day, it would seem that at least 1 percent or twenty boards should be tested. A good rule of thumb is that one to two boards taken at random out of each cleaned lot from a batch cleaner or one to two boards taken out of every hundred coming off an in-line one would seem a good compromise, no matter what the time scale. The frequency must be increased if the residual contamination levels are close to the limit or if a process change has been made, to make sure that the process cannot drift off the rails.

"Overnight" SIR testing is a secondary method that must gain in popularity. It is almost an essential process where no cleaning is carried out, as it is the only practical production method that permits production checking of the innocuity or otherwise of the residues which are left on the circuit for ever.

DEBUGGING

Where a problem occurs, any or many of the test methods mentioned earlier can be used to diagnose the cause. Once the cause has been found, the remedy is usually evident.

PROCESS CHECKING

This is almost a constant requalification procedure. The conscientious engineer must realise that the assembly/soldering/cleaning process is a delicate web of interacting parameters and a slight drift of any one of them may have unforeseen consequences. This may be illustrated by the fact that a change as low as 3°C of the

boards coming out of the preheater stage may, with some flux/cleaner combinations, render the post-solder residues uncleanable.

In practice, it means that sample boards should be regularly taken off the production lines and put through all the laboratory qualification procedures again. Ideally, this should be done on a quarterly basis but certainly not less frequently than annually. Many instrument users insist on an annual recalibration but they do not "recalibrate" their soldering machine or cleaning solvent.

CONCLUSIONS

Contamination testing is an essential part of high-reliability electronics. Many of the methods employed reflect the assemblies of when the standards were elaborated and which bear little or no relationship with modern electronics. Surface Mounting and cleaning without Ozone-Depleting solvents have both contributed to the development of modern instrumentation whose technical prowess has outstripped both the letter and the spirit of standards. That some of these latter need to be revised is well known and acknowledged and work is in progress but it must be admitted that the electronics industry, which should be progressive, is in reality often ultra-conservative, if only because there are frequently schools of thought that cannot reconcile themselves to a compromise with other schools—that none of them are right may never have crossed anyone's mind! The average length of time from the idea that a new standard needs to be written or an old one revised to the date of publication may take three, four, five, sometimes even ten, years. This internecine warfare, including the digging in of heels to retain obsolete processes no matter what the cost, is detrimental to the electronics industry, is extremely costly in manpower and cash and serves no useful purpose. "Reinvention of the wheel" is another sin in our industry: how many persons repeat the same experiments the world over, to obtain the same results? All this is mentioned, not because there is any hope of changing the situation on either side of the Atlantic or Pacific but simply to mention that some of both European and American manufacturers of contamination and SIR testers are well ahead of what the standards lay down, that there is a variety of models available ranging from simple low-cost manual ones to highly sophisticated computerised ones. Some of these instruments are truly "state-of-the-art" and bear little resemblance to what was available only a decade ago.

WARNING

It has been shown that process qualification for high reliability may take several months or over one year. Swiss and German CFC-113 and 1,1,1-trichloroethane phase-out regulations do not leave much time for this to be done correctly. It is strongly recommended that companies who have not yet started substitute qualification must do so immediately. At this moment, equipment manufacturers have spare capacity and will welcome orders for contamination testers and non-ozone-depleting process cleaning machines for delivery in ample time before the regulations come into force. A delay of another six months may find that the equipment manufacturers can no longer meet delivery schedules before the deadline. It is therefore imperative that manufacturers of high reliability electronics take steps now.

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RELIABILITY ASSESSMENT OF ANTIMONY REMOVAL FROM TIN-LEAD SOLDERS

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In 1957, the U. S. Military required tin-lead solders to maintain a level of antimony between 0.2 - 0.5%. This requirement was seen in Federal Solder Specification QQ-S-571C. The inclusion of a specified minimum antimony amount was controversial (ref. 1). Initially, the reason for a low level of antimony was to prevent tin pest. Tin pest is defined as the phase change of beta-tin to alpha-tin. This allotropic phase change results in a volume increase of 26% usually causing a disintegration of the metal into a powder. The process occurs at temperatures below 13° and is accelerated by application of tensile stress. Low levels of antimony were believed to suppress the phase change in tin-lead solders (ref 2). Although "tin pest" has been reported in tin-lead solders as a white powder on the surface of solder joints, no significant deterioration of a solder joint has been seen. High purity tin is indeed susceptible to tin pest. However, when high levels of lead or other impurity is present, tin pest is not known to occur (ref. 3).

Solders containing antimony began to receive more attention when auto-insert equipment became available to electronics manufacturers. This new technology required that the hole to lead ratios of hardware be increased. Strength improvements were needed to maintain high reliability especially in class 3 military systems (ref. 4). Data indicated that antimony-tin-lead solders provided this additional strength (refs. 3,5).

High levels of antimony were seen to cause problems with tin-lead solders such that an upper level was established. Decreases in wetting power (ref. 6) and area of wetting spread (ref. 7,8) are observed with low levels of antimony present although each of these effects can be overcome with the use of activated fluxes. If antimony is maintained at a level between 0.2 - 0.5%, significant decreases in wetting will not be found (ref. 9).

The mechanism of action of antimony is not clear. Tin will dissolve up to 7% antimony. When the antimony levels exceed this amount, an intermetallic of tin - antimony (SnSb) will precipitate out of solution as cubic crystals (ref. 10). Favorable effects of antimony addition, i.e., strength

increase of the solder joint, is most likely caused by the ability of the metal to slow oxidation of molten solder (refs. 3, 11) and eliminate undesirable impurities such as aluminum (ref. 3) by forming inert intermetallics. Low levels of aluminum are known to accelerate the oxidation of molten solder which results in weakened solder joints as well as the formation of icicles and bridges (ref. 9).

Although much of the reported data on antimony addition to tin-lead solders has been controversial and sometimes contradictory, the military decided to maintain minimum levels of this metal. This material has been available in plentiful supply and was less expensive than tin. Recently however, the supply of antimony has been threatened. Most of this element is provided to the world from one supplier, China. Because of the political situation developing in that country, the U. S. Department of Defense no longer considers antimony to be readily available. To address this potential problem, Federal Solder Specification QQ-S-571E, Interim Amendment 6 (ER), has eliminated the minimum amount of antimony required in tin-lead solders. The new requirement simply states that tin-lead solders are acceptable for military use if the antimony levels are maintained between 0.0 - 0.5%. Because of the controversy surrounding this requirement, a study was undertaken to determine if there would be a significant decrease in reliability of military electronic hardware if all antimony were removed from tin-lead solders.

In an effort to gather as much data as possible in a short period of time, the decision was made to subject solder joints made with antimony and without antimony to as harsh of conditions as possible and compare the effects. To this end, Naval Weapons Center Soldering School Printed Wiring Boards seen in figure 1 were assembled. Each board contained plated through hole and surface mount components as well as wires for strength pull testing. Six boards using solder containing antimony and six boards using antimony free solder were used. Inductively-coupled argon plasma analysis determined each solder to have the following composition: 0.3% antimony, 61.29% tin, remainder lead; 0.04% antimony, 62.05% tin, remainder lead. The printed circuit boards were hand soldered and visually inspected as per Mil-Std-2000. All joints passed inspection. Typical examples of the solder connections are seen in figures 2 and 3. Figure 2 shows the joints of a dual-in-line package (DIP) using solder without antimony. Figure 3 is also a DIP solder joint which contains antimony. There was no visual difference between the two connections. Each joint appeared as bright and shiny. There was good wetting with well formed fillets. The boards were subjected to thermal cycling in accordance with Mil-Std-883, Notice 5, Method 1010.7, condition B for 250 cycles. One cycle consisted of step 1 at -55°, +0/-10° C followed by step

2 at 125°, +15/-0° C. Dwell time at each step was not less than 10 minutes with the specified temperature being reached within 15 minutes. Two separate temperature chambers were used with the samples being transferred by hand. The average time to reach the dwell temperature was less than three minutes.

After exposure to 250 cycles the assembled boards were examined. All solder joints had changed from a smooth bright shiny surface finish to a grainy non-uniform condition. Surface cracks had appeared in a majority of the fillets. Because of the obvious stress, the thermal cycling was stopped. Figure 4 shows connections containing no antimony and figure 5 shows connections which have antimony. There was no clear discernable difference between the two different types of solder. Surface cracks and grainy appearance were present to the same degree in each type of joint. Figures 6 and 7 show optical photographs of magnified microsections of plated through hole solder joints of connections with and without antimony respectively. The magnification in each is 800X. Each joint appeared as nearly identical. Examination of each microsection shows an increased separation of the tin and lead phases with a significant amount of porosity. The thermal cycling induced considerable stress to each type of joint. Although the stress was obvious, it is important to note that there was no evidence of large cracks appearing in the bulk of the joint or dewetting of the solder. The observed surface cracking did not extend into the joint. Presence or absence of antimony had no effect on how the connections reacted to the thermal cycling.

Figures 8 and 9 show scanning electron microscope (SEM) micrographs of plated through hole microscections without and with antimony respectively. In each joint two small cracks were evident. Since each crack appears in the same place, and these cracks were seen only in one type of connection (resistors soldered to ground planes), we believe that this is an indication of the joint configuration rather than the physical properties of the solder. No other component connection exhibited this type of cracking. Further high magnification SEM examination of the thermally cycled joints is seen in figures 10 - 13. Figures 10 and 12 show joints with no antimony, 11 and 13 are joints with antimony. Size and distribution of the lead-rich phase in comparison to the tin-rich phase appeared to be the same in each joint. None of the joints showed evidence of any cracks extending into the bulk of the solder. Again, antimony was seen to have no effect on the solder's thermal cycling behavior.

Because of the importance of strength of solder in surface mount technology, we also examined the joints of a typical flat pack component. For reference, figure 14 shows the SEM micrograph of a microsectioned flat pack lead using

solder containing no antimony before thermal cycling. This micrograph was identical to flat pack joints containing antimony. As with plated through hole components, all of the solder joints, regardless if antimony was present or not, were smooth, shiny, and displayed good wetting on all fillets. After temperature cycling, the flat pack joints had a grainy appearance with evidence of surface cracking. SEM micrographs of joints without and with antimony are shown in figures 15 and 16 respectively. In each microsection there is no evidence of dewetting or cracks extending into the joint. Figure 17 and 18 show high magnification SEM micrographs of flat pack solder joint microsections after thermal cycling without and with antimony respectively. The appearance of these connections was almost identical with the plated through hole joints. The size and distribution of the lead-rich and tin-rich phases are similar as well as the porosity of the solder. As before, antimony had no effect on the physical changes induced in the solder from the thermal stress.

Six wires, 24 gauge, were also soldered to each board. Prior to temperature cycling, two wires were pulled from each board using an Orthodyne Electronics bond pull tester. The failure mode of each wire was breakage of the wire, not the solder joint. After cycling, the remaining wires were pulled. Unfortunately, the mode of failure in each test was also breakage of the wire. No quantitative strength data could be collected. However, it is clear that there was no gross difference between the two types of solder, nor was there a catastrophic failure of the non-antimony solder.

In an effort to induce tin pest, one board containing each type of solder was stored at -40°C for 500 hours. After this long term storage, each joint was examined optically. Although grain patterns were more evident in all of the joints, no tin pest was observed. No difference was seen between the two types of solder.

Shear strength was also measured for each solder type. In accordance with ASTM D1002, solid copper coupons measuring 1 inch wide by 4 inches long and 1/8 inch wide were solder dipped and vapor phase reflowed together with a one-half inch overlap. Ten test specimens of each of the two solders were assembled. The samples were not thermally cycled. Test results showed an average strength of 3990 psi for solder without antimony, and 3920 psi for solder containing antimony. While we do not consider this difference significant, the results indicate that in shear strength, antimony may weaken a solder joint.

The conclusion from these observations must be that small amounts of antimony have little or no significant effect on the properties of SN62 solder. We would predict

from our results that there should be no significant decrease in the reliability of soldered electronic assemblies by the reducing the minimum amount of antimony required in QQ-S-571. Although our testing revealed no significant difference between two types of solder, it would be worthwhile to extend this work further. Other tin-lead solder compositions should be examined to confirm our results thus far. Also, long-term reliability should be determined by simulated aging. Data on solder joint creep would also be useful.

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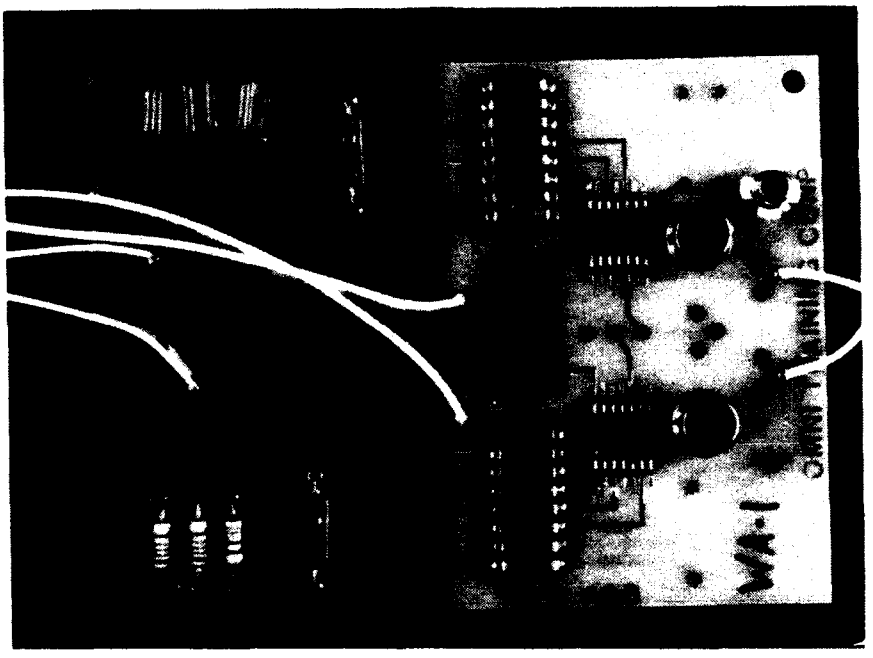

Figure 1. Printed wiring assembly used in this study.

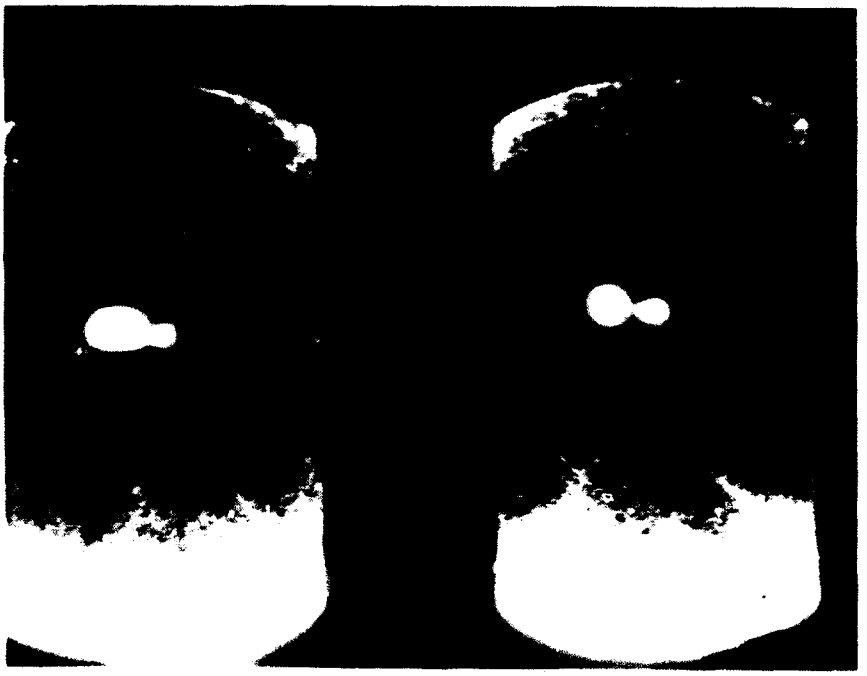

Figure 2. Appearance of a representative antimony free solder joint prior to thermal cycling magnified 32X.

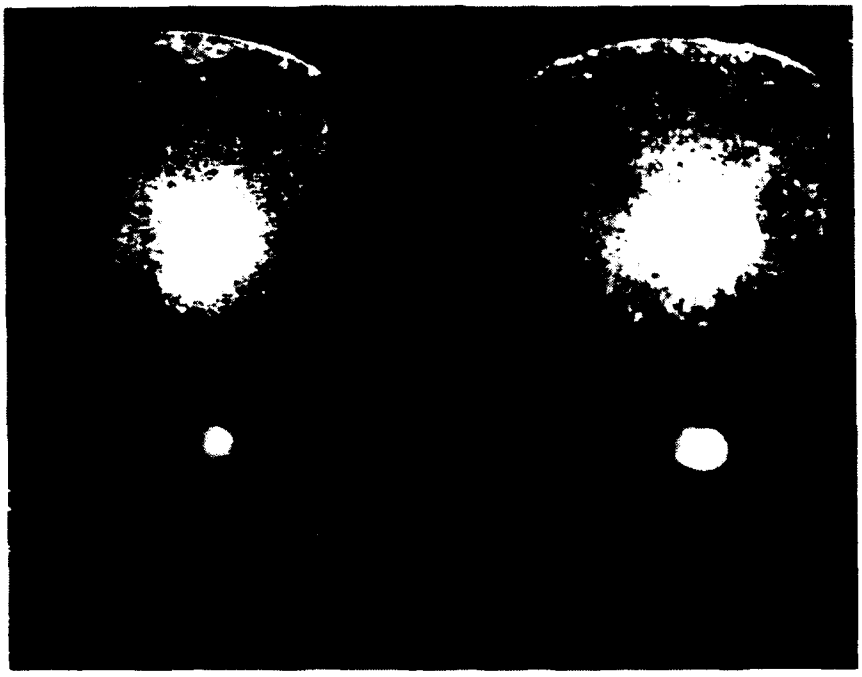

Figure 3. Appearance of a representative solder joint containing antimony prior to thermal cycling magnified 32X.

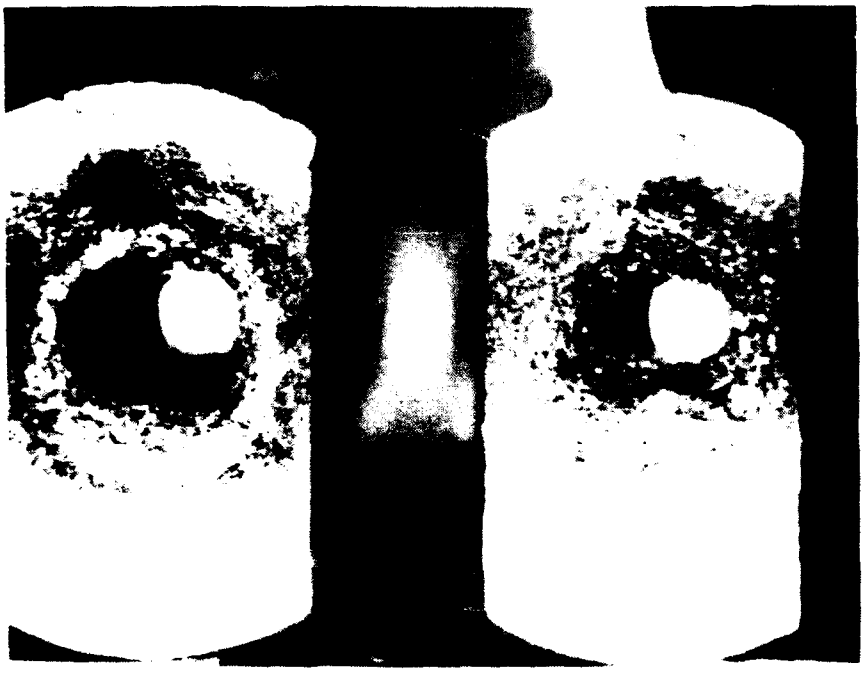

Figure 4. Antinomy free solder joint after 250 thermal cycles magnified 32X.

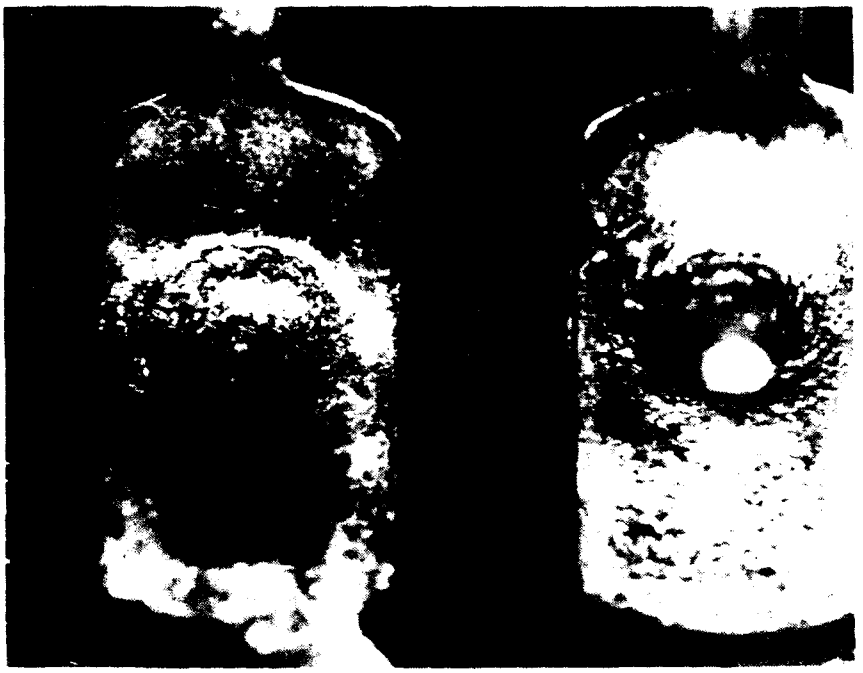

Figure 5. Solder joint containing antimony after 250 thermal cycles magnified 32X.

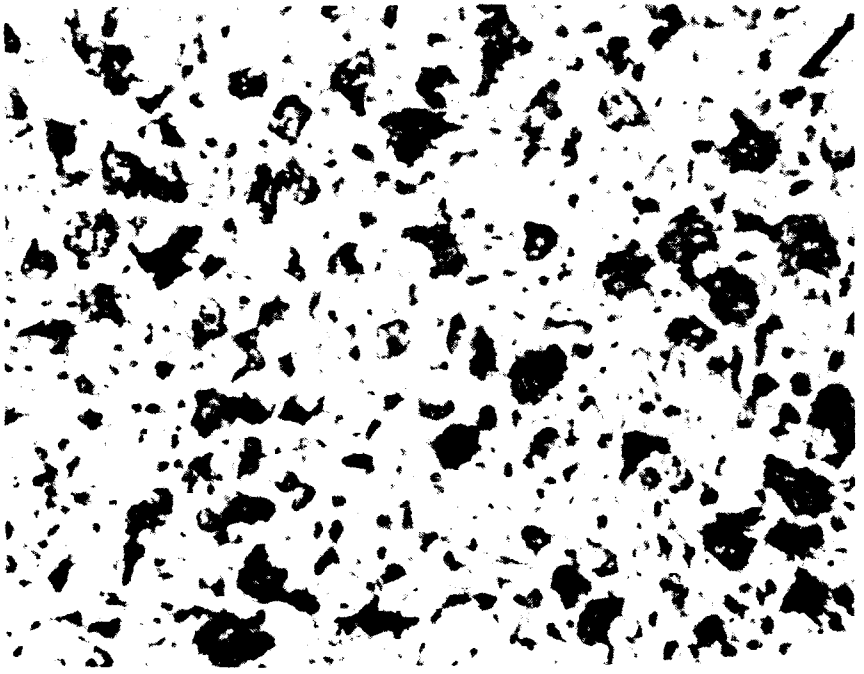

Figure 6. Optical photo of microsection of solder joint with antimony after 250 thermal cycles magnified 800X.

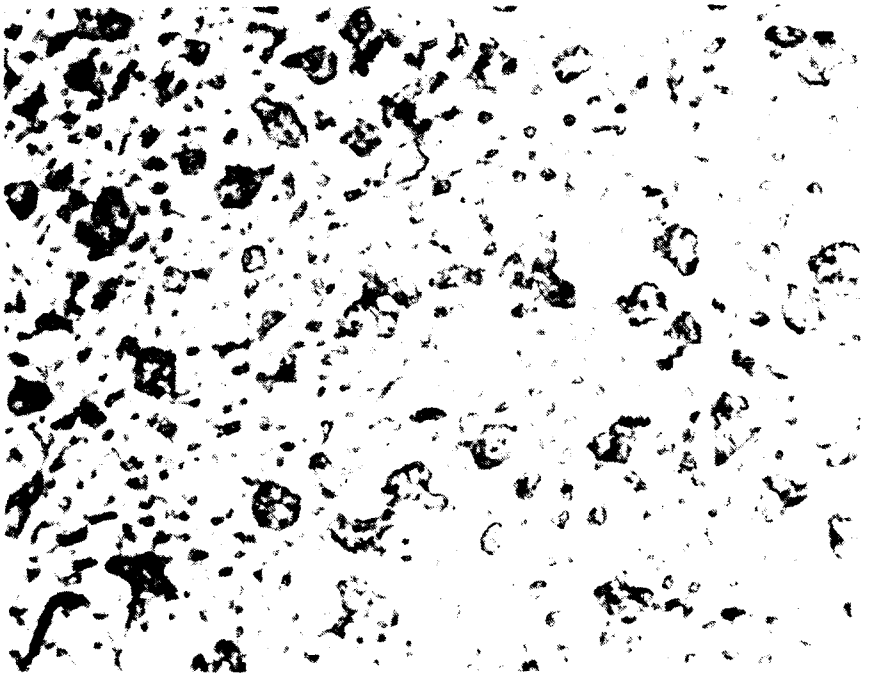

Figure 7. Optical photo of microsection of antimony free solder joint after 250 thermal cycles magnified 800X.

Figure 8. SEM micrograph of a microsectioned antimony free solder joint after 250 thermal cycles magnified 26X. Arrows indicate cracks in solder.

Figure 9. SEM micrograph of a microsectioned solder joint containing antimony after 250 thermal cycles magnified 30X.

Figure 10. SEM micrograph of a microsectioned antimony free solder joint after 250 thermal cycles magnified 1300X.

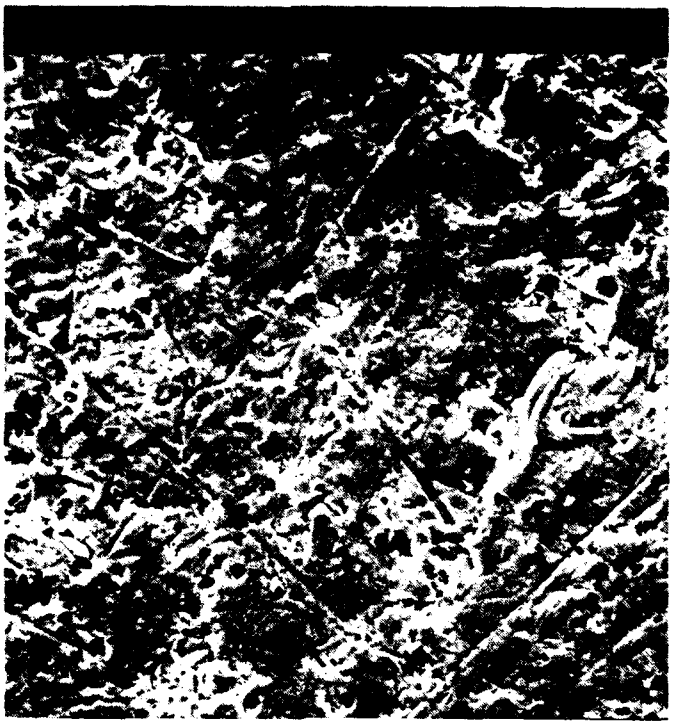

Figure 11. SEM micrograph of a microsectioned solder joint containing antimony after 250 thermal cycles magnified 1200X.

Figure 12. SEM micrograph of a microsectioned antimony free solder joint after 250 thermal cycles magnified 3000X.

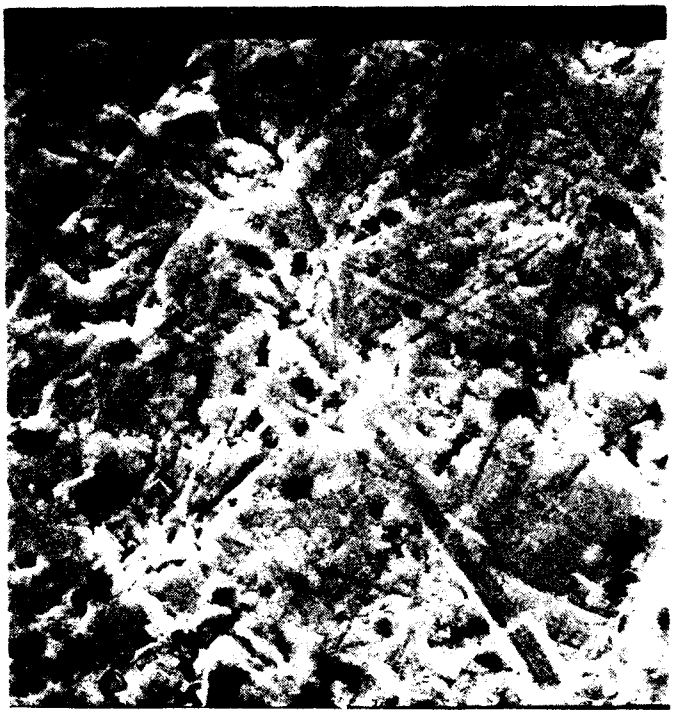

Figure 13. SEM micrograph of a microsectioned solder joint containing antimony after 250 thermal cycles magnified 3000X.

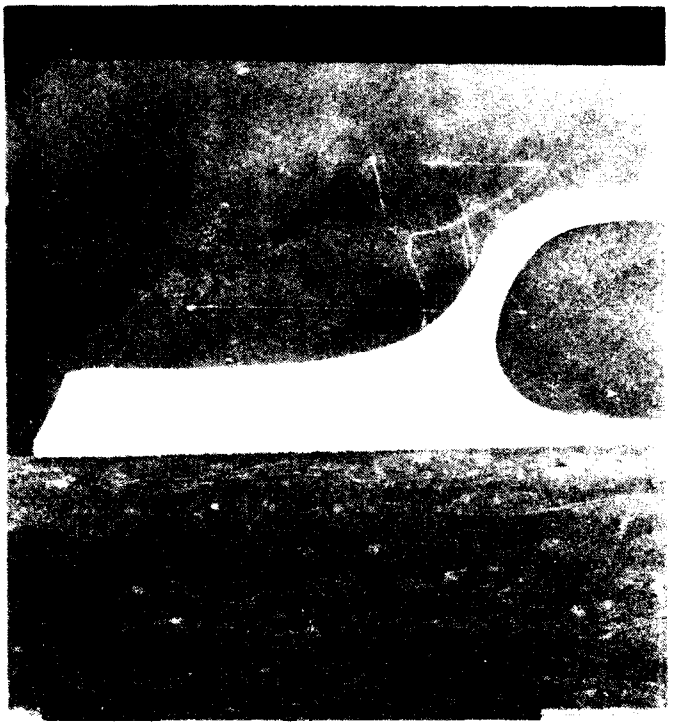

Figure 14. SEM micrograph of a microsectioned antimony free flat pack solder joint magnified 30X.

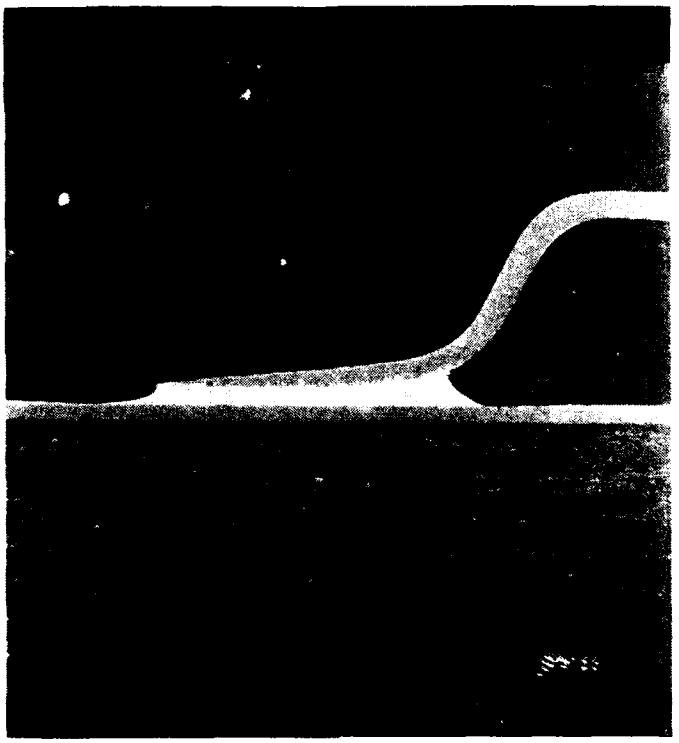

Figure 15. SEM micrograph of a microsectioned antimony free flat pack solder joint after 250 thermal cycles magnified 24X.

Figure 16. SEM micrograph of a microsectioned flat pack solder joint containing antimony after 250 thermal cycles magnified 24X.

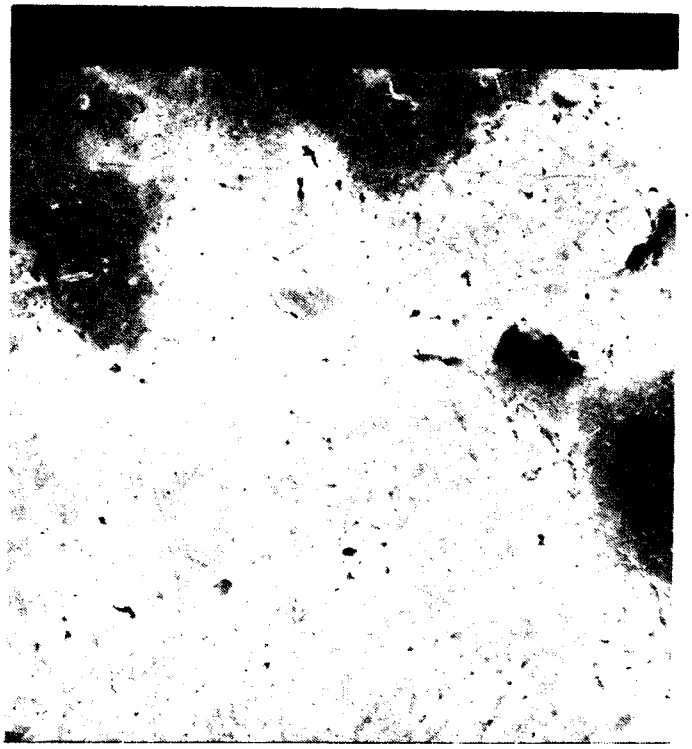

Figure 17. SEM micrograph of a microsectioned antimony free flat pack solder joint at the heel after 250 thermal cycles magnified 1200X.

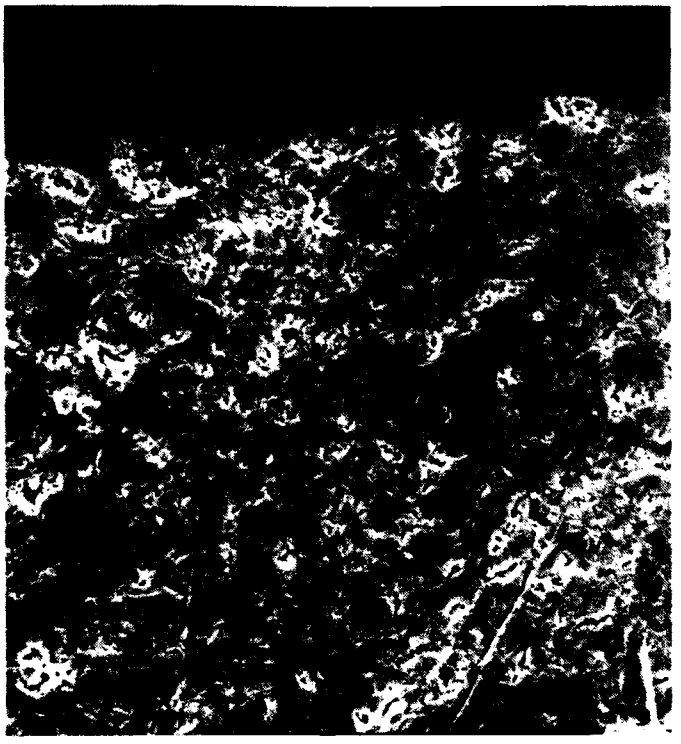

Figure 18. SEM micrograph of a microsectioned flat pack solder joint containing antimony after 250 thermal cycles magnified 1200X.

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The Relationship of Component Solderability Testing to Board Level Soldering Performance

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ABSTRACT

Visual inspection remains the dominant method of assessing component lead solderability and finished board solder joint quality. In recent years the wetting balance has received much attention as an attractive alternative to the inherently subjective visual inspection method of assessing component termination solderability. Regardless of which method is used, either direct visual inspection or wetting balance methods, the results must be in agreement with board level soldering performance to be effective.

This paper addresses the issue of the agreement of visual board level solder joint quality with both visual " dip and look " solderability assessment and wetting balance measurement of the components prior to board assembly. A description of visual "dip and look" solderability test assessment along with wetting balance methodology for components is presented in Section 1. A compendium of wetting balance tests and indices are documented in the Appendix. Section 2 outlines the experimental strategy employed while Section 3 details the experimental technique including the equipment, materials and component sample preparations. The experimental results, given in Section 4, present a comparison of both "dip and look" visual solderability assessment and wetting balance measures to actual board level soldering performance. Section 4 also explores the capability of the various assessment methods to predict board level defects. Conclusions and recommendations are summarized in Section 5.

1. BACKGROUND

In recent years increased emphasis has been placed on the use of solderability testing of electronic component terminations to ensure that component terminations are solderable when received and will remain so after extended storage. In order to achieve a 100 ppm defect rate at board level soldering operations it is imperative that the component terminations be highly solderable.

Currently, the most widely accepted methods for assessing component termination solderability are "dip and look" tests. Various military standard solderability test methods (883/2003, 202/208, 750, and STD-2000) and industry standard test methods (IEC-68-2, EIA-IS49, and IPC-805) specify a visual inspection accept/reject criteria of 95% solder coverage of the component termination being tested after exposure to specified stressing conditions (such as 8 hours of steam aging).

Considerable work has been done comparing the "dip and look" solderability test performance of various component terminations lead finish types (see, for example, Wild[9]). Solderability test performance as a function of steam age stressing conditions of time and temperature has been, and continues to be, an active topic of lead finish research. Moreover, a significant improvement in solderability has been realized during the last five years with the use of longer steam age times in conjunction with the "dip and look" tests mentioned above. When these tests are quoted in procurement specifications the overall result has been a higher quality of component lead solderability supplied by component manufacturers to the board level assembly houses.

However, the "dip and look" tests require visual estimation (typically at 10X magnification) or exact measurement of the 5% allowable nonconformal areas. The subjectivity in this estimation is the essence of the controversy over the discriminating ability of these tests. For instance, Wolverton[10] has documented large within and between inspector variabilities associated in the visual estimation of 95% solder coverage on leaded component terminations.

Achieving reproducibility of solderability testing results presents a challenge to the current "dip and look" assessment techniques. As a result, it is often difficult to strictly control the quality of the lead finish entering the board level assembly houses. It is not uncommon for perfectly good, solderable components to be rejected while marginally solderable or marginally unsolderable components are accepted. This can potentially result in costly line shutdowns, production disruptions, increased component costs due to unnecessary handling or engineering dispositions, supplier arguments, or costly solder joint rework on boards with the liability of poor quality solder joints present in the finished assembly. As an alternative, the wetting balance

shows promise as a technique of quantifying the solderability of component lead terminations and reducing the variability associated with the "dip and look" techniques.

Wetting Balance Methodology

The wetting balance is an instrument that measures the "weight gain" of a material being immersed in molten solder as the solder "wets" and alloys to it. Figure 1 shows a typical wetting balance curve along with the notation used in this paper for curve time, and force coordinates. From Figure 1, it is evident that as the termination (wire or lead) is immersed into solder, it experiences a buoyant force (in gram-force units) from the displaced solder. Since the termination is "lighter" due to this buoyant force, a "negative weight" is registered by the transducer as the wetting balance curve plunges below the zero line from point 0 to point 1 in Figure 1.

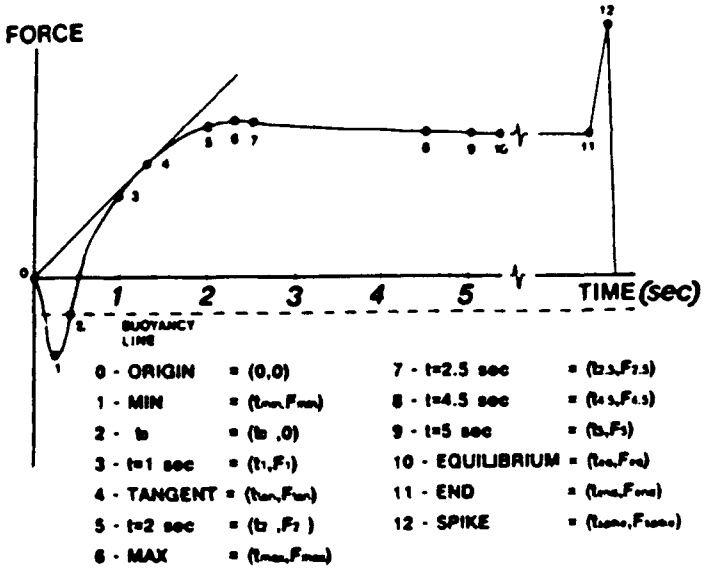

FIGURE 1. Typical wetting balance curve.

As the solder begins to wet onto the termination, the buoyant force is counter balanced by the weight of solder alloying with the termination in point 2 in Figure 1. Typically, when testing a solderable termination, the solder will continue wetting well past the zero force line (point 2 to point 4 in Figure 1) and will then begin to gradually approach a maximum value (point 4 to point 6).

Sometimes a loss in weight (point 6 to point 11) is observed after the maximum wetting force is obtained. This condition is indicative of unstable wetting or dewetting (DeVore [3]). At the end of the test the termination is removed from the solder and the inertia during withdrawal is displayed as a large weight gain (points 11 and 12 in Figure 1).

Intuitively, highly solderable terminations should exhibit wetting curves indicative of fast initial wetting, i.e. the wetting curve should soon recross the zero force line reflecting the rapid counter balance of the wetting force to the buoyant force of the termination in the solder. Next, highly solderable terminations should have a very steep wetting balance curve from point 2 to point 5 in Figure 1 owing to the rapid alloying to the basis metal of the termination. In addition, stability of wetting will be exhibited by a wetting curve maintaining a large maximum force throughout the test.

Conversely, terminations with poor solderability may be expected to exhibit longer times to counter balance the buoyant force and should have a lesser wetting curve slope as testing progresses. In fact, some unsolderable terminations may not even recross the zero force line.

To quantify properties of wetting balance curves many authors (see, for example, [1-3,6,7,11]) have proposed specific wetting balance indices for assessing solderability. These wetting balance indices offer the potential to objectively assess the solderability of electronic component terminations. Besides being able to predict solder coverage on component terminations with wetting balance indices, it would be clearly advantageous to know what kind of wetting balance properties are inherent to terminations exhibiting measurable soldering defects after board level assembly soldering.

The Appendix contains a brief description of standard wetting balance indices and tests including DeVore's solderability index (SI), DeVore's coefficient of wetting (CW), stability of wetting index (SW), percent of theoretical maximum force attained ($PCTF_{th}$), an industry standard solderability test (ISTD), MIL-STD-883/TM2022 (TM2022), and Wooldridge's modified 883/2022 method (MOD2022). In addition, the Appendix defines four indices proposed by Mullenix, Gerke and Kwoka [6] known as angle to maximum wetting force (MAXANG), adjusted attained maximum wetting force ($ADJF_{max}$), adjusted theoretical wetting force ($ADJF_{th}$) and the attained wetting force range (F_{range}).

2. EXPERIMENTAL STRATEGY

The experimental strategy was to create experimental test components exhibiting a wide range of wetting performance from "good" to "bad" as measured by both wetting balance and visual inspection criteria. This range of wetting performance was obtained by pretreating the experimental components with various cleaning methods described in Section 3. Both the cleaning time and the orientation of the units within the bath were varied. The format of this cleaning matrix is recognizable as a fractional factorial design. A discussion of this cleaning matrix and the effect of the cleaning factors on the solderability of the test components is beyond the scope of this paper. This subject will be elaborated upon in a future publication. It is sufficient to know that the use of this cleaning matrix and the associated burn-in conditions produced experimental test units that exhibited the range of wetting performance that we were trying to obtain.

After the experimental units were prepared, measurements of the wetting balance parameters and indices mentioned above were performed. In this study the wetting balance measurements were taken on the component or unit level (all leads are dipped at the same time), rather than on the individual lead level. This type of wetting balance testing does not allow identification or accounting of the within unit (lead to lead) variability in the wetting balance measures. After the wetting balance measurements were completed, each unit was visually inspected for solder coverage. The visual inspection data was summarized by unit for each 18 lead ceramic dual in-line package (CERDIP) in the study. The visual inspection for defects was performed at 10X magnification and a visual estimation of the percent solder coverage on the leads was recorded for each test component.

To facilitate the visual inspection, components were classified into five coverage categories; viz., 0 - 24%, 25 - 49%, 50 - 74%, 75 - 94%, and 95 - 100% coverage. Further, the associated lead finish defects were recorded and classified as either no-defect, asperous, dewet, pinhole or nonwet.

Finally, these same test components, for which the wetting balance and visual inspection data had been previously recorded, were soldered into a circuit board using "standard" wave soldering parameters (which will be given in the next section). After soldering and cleaning were complete, the resulting solder joints were visually inspected at 10X to 30X magnification.

Each solder joint was classified into one of five solderability categories: C1 = no visible defect according to MIL-STD-2000 section 4.19.5.1; C2 = acceptable per MIL-STD-2000 section 4.19.5.1 but some (less than 5%) dewet/nonwet visible; C3 = rejectable per MIL-STD-2000 section 4.19.5.1. with more than 50% wetting/filleting

on joint; C4 = rejectable per MIL-STD-2000 with less than 50% wetting/filleting on joints and some wetting/filleting visible; and C5 = rejectable per MIL-STD-2000 and no evidence of wetting/filleting.

In addition, the number of holes not filled completely for each component was recorded. This data was not taken using the requirements of MIL-STD-2000 since inspection views were sometimes cramped and it was easier to discern whether a hole was filled or not rather than determine the percentage of the board thickness that was exhibited by a given solder recession.

The ultimate objective was to find wetting performance measures which would be predictive of board level soldering performance. Both the current and proposed indices by the authors (see the Appendix) were examined for association with board level soldering performance. Due to the absence of published work on this specific issue of solderability test correlation with board level soldering performance, the authors made no attempt to replicate the experimental runs/inspections used in this first study in order to determine the amount of variability associated with the visual inspections of the component leads, finished solder joints or lead to lead variabilities associated with the wetting balance measurements. This type of replication might be of interest as a future research topic. Only after the relationship between wetting balance indices and board level soldering performance is understood can a meaningful solderability test be developed with appropriate "guardbands" to ensure good board level performance and minimize the rejection of good, solderable parts.

3. EXPERIMENTAL TECHNIQUE

A total of 322, 18 lead, ceramic dual in-line packages (CERDIP's) were sealed with no die in the packages. These parts were then split into seven groups of 46 units per group and individually labeled. Each group was then submitted for lead finish preclean processing as listed in Table 1 below.

The groups were then moved on to either matte tin electroplate or hot solder dip lead finish application. The matte tin plating was applied using a standard "Wren" type stannous sulfate acid plating bath with Janus Green B, Igepal and Hydroquinone additives. Hot solder dip lead finish was applied using a Hollis TDL-12 wave solder machine and the following conditions: preheat temp = 100 degrees C; conveyor speed = 9 ft/min; flux = Kester 2161 O.A.

TABLE 1. Cleaning Methods

Group	Orientation	Time
1	Stacked	4 min.
2	Singulated	2 min.
3	Singulated	0.5 min.
4	No Clean	
5	Singulated	4 min.
6	Stacked	2 min.
7	Stacked	0.5 min.

After lead finish application, three units from each group were wetting balance tested using type R flux. The wetting balance parameters described in the Appendix were taken from the wetting balance curve generated for each unit tested.

For the purposes of this paper all wetting balance measurements are given in force per unit distance (μN/mm) by adjusting for buoyancy and perimeter with the formula

$$F_{(corrected)} = (\text{observed gram-force measurement} + F_b)/p$$

in which p is the perimeter of the unit's cross section coplanar with the solder surface, and

$$F_b = \rho\, g\, V$$

is the buoyancy force with ρ = density of molten solder (8.155 g/cm^3 for Sn63 solder), g = acceleration due to gravity (980 cm/sec^2), and V = volume of solder displaced by the component termination during immersion.

These same units were subsequently visually inspected for solder coverage and lead finish defect category at 10X magnification. To achieve a more standardized inspection, each unit was inspected and categorized according to the five coverage categories and five defect categories stated previously in Section 2.

To stress some of the units in an attempt to create a wide range of solderability performance, the remainder of each group was then split with half of each group submitted to a 168 hr burn-in at 125 degrees C per MIL-STD-883 and the other half of each group subjected to 424 hrs of burn in at 125 degrees C. After burn-in was complete, three unit samples were pulled from each burn-in subgroup and wetting balance tested using type R flux. Each unit was subsequently visually inspected at 10X magnification. To summarize this process, a flowchart is given by Figure 2.

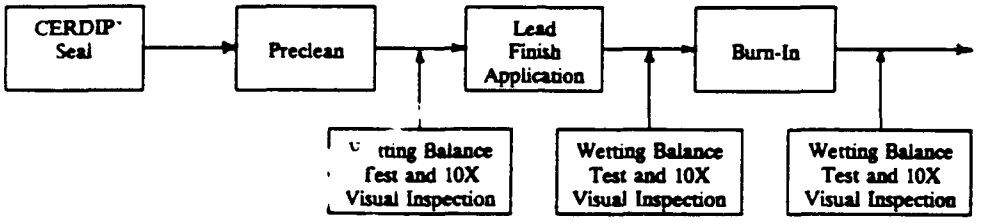

FIGURE 2. Experimental process flow diagram.

Following wetting balance testing and visual inspection at 10X, 36 units were selected from among the seven groups. The selection criteria aimed at choosing a sufficient number of units from each visual inspection-solder coverage category to allow for a meaningful statistical comparison.

The 36 units were then soldered into a multilayer board using an Electrovert Ultrapak 445 wave solder machine. The board level soldering conditions used in this study were those published by Wooldridge[12]: solder temperature = 260 degrees C; topside board preheat temperature = 100 degrees C; conveyor speed = 1.9 ft/min; and Alpha 611 RMA flux. The soldered board was post cleaned using isopropyl alcohol/ultrasonic cleaning for five minutes followed by a freon ultrasonic cleaning for five minutes, a freon spray cleaning for one minute and finally a freon vapor degreasing for five minutes. After cleaning was completed, all of the 648 solder joints on the 36 units were visually inspected at 10X - 30X magnification. Each joint was classified into one of the five visual inspection coverage categories given in Section 2.

4. EXPERIMENTAL RESULTS

To facilitate assessment of the association between both visual "dip and look" tests and wetting balance solderability assessment with visual board level soldering performance, a scoring function was developed.

First, each of the 36 CERDIP 18 lead units in the study, was visually inspected after being soldered into a circuit board. The solder joints formed on the leads of each unit were then classified into five visual categories, C1, C2, C3, C4 and C5 (see Section 2). The visual categories represent gradations in solder joint visual appearance from C1 = "no visible defect" to C5 = no evidence of wetting/filleting.

This provides a categorization at the lead-joint level. To obtain a visual board level soldering performance category for each unit, the scoring function uses a weighted average of number of lead-joints in each lead-joint visual category. This scoring function is specific to the units under study and may not be suitable for general use. It is used here as a logical means of classifying units for board level soldering performance in order to make comparisons to "dip and look" solderability assessment categorizations. The form of the scoring function used is

$$\text{unit score} = n(C1) + 2*n(C2) + 20*n(C3) + 40*n(C4) + 80*n(C5)$$

where n(category) denotes the number of leads classified in the given category.

Note from the coefficient weights that low unit scores are desirable and unit scores may range from 18 (all 18 leads in category C1) to 1440 (all 18 leads in category C5). Unit scores falling in intermediate ranges are classified in Table 2 into the board level soldering performance categories denoted A, B, C, D and E.

TABLE 2. Board-level Soldering Category Classification

Board-level Soldering Performance Category	Unit Score Range
A	18 - 22
B	23 - 36
C	37 - 360
D	361 - 720
E	721 - 1440

This scoring function with "relative weights" for each category of joint classification are arbitrarily chosen by the authors based on "engineering judgement." However, upon inspection, the results are consistent and seemed to provide a realistic categorization of units into the board visual categories A - E. With further experimentation this technique could be refined into a more rigorously developed classification scheme.

Table 3 below presents a cross-tabulation of the unit board soldering performance grouping with the "dip and look" defect categories of no defect, asperous, pinholes, dewetting and nonwetting. From Table 3 we see that board soldering performance categories A and B are indistinguishable on "dip and look" defect category. However, board soldering performance categories C - E display a nonwetting behavior on the "dip and look" test. Kendall's tau-b of 0.706 shows that there is a relatively strong association between board score category and the "dip and look" defect categories.

TABLE 3. Unit Board Soldering Performance Versus "Dip and Look" Defects

"Dip and Look" Defect Category	Board Score Category Best → Worst				
	A	B	C	D	E
Asperous	2	2	1	0	0
Pin Holes	4	4	1	0	0
Dewetting	0	0	1	0	0
Non-Wetting	0	0	8	1	12
Kendall's Tau-b = 0.706					

Table 4 gives the same comparison as Table 3 at the lead level, i.e. the number of leads in categories C1 - C5 is cross-classified by unit defect category. The same general association of non-wetting on the "dip and look" with poorer board soldering performance is observed.

TABLE 4. Lead-Joint Board Soldering Performance Versus "Dip and Look" Defects

"Dip and Look" Defect Category	Board Lead-Joint Category Best → Worst				
	C1	C2	C3	C4	C5
Asperous	69	19	1	1	0
Pin Holes	117	44	0	1	0
Dewetting	6	9	3	0	0
Non-Wetting	10	34	115	19	200

Table 5 shows a similar cross-tabulation of board soldering performance grouping with the "dip and look" coverage categories of 0-24%, 25-49%, 50-74%, 75-94% and 95-100%. Again board soldering performance categories A and B appear indistinguishable, each having three units in both the 75-94% and 95-100% categories. The visual coverage performance of categories C - E degrades steadily. Kendall's tau-b of 0.806 again shows a strong association. Similar to Table 4, a comparison of "dip and look" coverage categories with number of leads in each board soldering performance category is given in Table 6. Here the degradation in visual coverage is apparent for all groups C1 - C5.

TABLE 5. Unit Board Soldering Performance Versus "Dip and Look" Coverage

"Dip and Look" Coverage Category	Board Score Category Best → Worst				
	A	B	C	D	E
95 - 100%	3	3	1	0	0
75 - 94%	3	3	2	0	0
50 - 74%	0	0	7	0	1
25 - 49%	0	0	1	1	2
0 - 24%	0	0	0	0	9
Kendall's Tau-b = 0.806					

TABLE 6. Lead-Joint Board Soldering Performance Versus "Dip and Look" Coverage

"Dip and Look" Coverage Category	Board Lead-Joint Category Best → Worst				
	C1	C2	C3	C4	C5
95 - 100%	97	27	1	1	0
75 - 94%	95	45	3	1	0
50 - 74%	5	28	90	3	18
25 - 49%	5	4	24	9	30
0 - 24%	0	2	1	7	152

Table 7. Correlations of Wetting Balance Indices with Number of Holes Not Filled (NHNF)

Solderability Index	n	Correlation with NHNF	p-Value
MAXANG	28	-0.781	0.0001
CW	6	-0.974	0.0010
$PCTF_{th}$	28	-0.530	0.0031
$ADJF_{th}$	23	-0.436	0.0375
SW	28	-0.317	0.0940
$ADJF_{max}$	23	0.196	0.3691
SI	23	-0.179	0.4140
F_{range}	26	0.099	0.6294

Table 8. Correlations of Wetting Balance Parameters with Number of Holes Not Filled (NHNF)

Solderability Parameter	n	Correlation with NHNF	p-Value
F_{spike}	28	-0.704	0.0001
$F_{(1)}$	26	-0.687	0.0001
$F_{(2)}$	26	-0.647	0.0003
F_{min}	25	-0.579	0.0020
F_{max}	28	-0.525	0.0034
F_{end}	28	0.497	0.0061
$F_{(5)}$	26	-0.441	0.0212
F_{tan}	23	0.135	0.5387

Another measure of the board level soldering performance is the number of holes not filled (NHNF). To evaluate the relationship between NHNF filled and solderability indices, correlations are computed. The only highly significant non-zero correlations found with NHNF are DeVore's coefficient of wetting, CW, and the authors' MAXANG, both described in the Appendix. Table 7 summarizes these correlations along with the sample sizes and approximate observed significance levels. Table 8 provides similar information for correlations between NHNF and solderability force parameters. Almost all the correlations are negative, which one might expect, i.e. the larger the wetting balance force measurement, the fewer holes not filled are found at board soldering. Although several of the correlations are significantly non-zero, none appear to have exceptionally high predictive value.

Using the method of discriminant analysis discussed by the authors[6, 7], canonical discriminant functions are developed which may be used for predictive purposes to classify observations into board visual categories A - E (note that no parametric information on units from groups D was available since these units failed to wet and hence did not register on the wetting balance). Either wetting balance indices or force parameters may be used for discriminant analysis. However, with the advent of software capable of sampling the wetting balance curve at frequent intervals, wetting balance force parameters are easier to deal with than solderability indices. Consequently, the parameters of time and force are taken directly from the wetting balance curves for the development of discriminant functions.

Table 9. Standardized, Total Structure and Raw Canonical Coefficients

Parameter	Canonical Coefficients					
	Standardized		Structure		Raw	
	Fn1	Fn2	Fn1	Fn2	Fn1	Fn2
F_{min}	0.53	-2.90	0.84	-0.16	0.01	-0.07
F_{max}	-2.07	-1.93	0.68	-0.33	-0.01	-0.01
F_{end}	-0.86	-4.28	0.60	-0.38	-0.01	-0.03
F_{spike}	1.12	4.06	0.76	-0.15	0.01	0.04
$F_{(1)}$	2.06	1.52	0.89	0.03	0.02	0.01
$F_{(2)}$	-1.95	1.30	0.84	-0.20	-0.02	0.01
$F_{(5)}$	3.79	1.10	0.75	-0.32	0.03	0.01

The standardized canonical coefficients, total structure coefficients and raw canonical coefficients for two discriminant functions describing board visual categorization from wetting balance parameters are listed in Table 9.

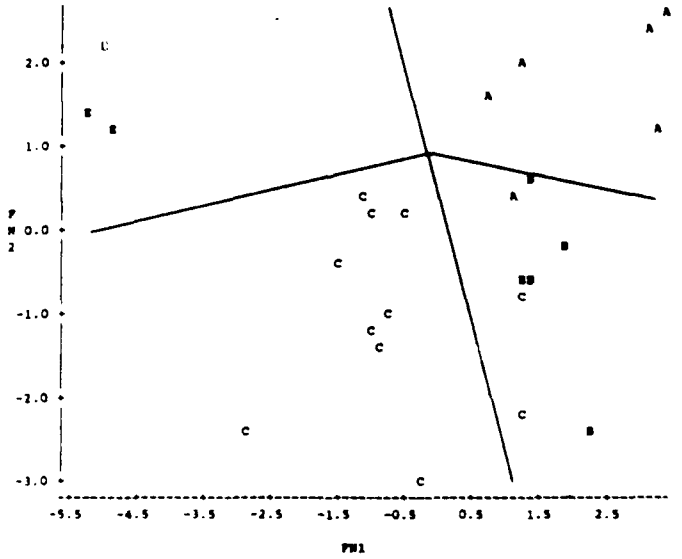

FIGURE 3. Canonical function region with board visual score category as symbol plotted.

Figure 3 gives the canonical function region for the board visual categories A -E. The figure illustrates regions in which the various board visual scores cluster. In practice, discriminant functions could be determined which would classify units real time into board visual categories. It is important to note that in this study only three units from the validation half of the data were incorrectly classified using this discriminant function method.

Besides relating performance on wetting balance indices and parameters to board level soldering performance, many are also concerned with the association of current solderability tests with board level soldering performance. Table 10 gives a comparison of solderability test results on predicting board visual score category (A-E) for the solderability tests TM2022, MOD2022, and ISTD along with tests based on the wetting balance parameters F_{spike}, F_{max}, and $F_{(2)}$.

It is easily seen from Table 10 that some of the existing solderability test methods are overly restrictive. For example, of the six units tested by solderability test TM2022 five of the six were rejected, yet all six units exhibited category A board-level soldering performance. Similarly, of the six units displaying category A board-level performance tested using test method ISTD, again five of the six units failed the solderability test requirements. The solderability test method MOD2022 is somewhat better in this regard. However, all three of these solderability tests in general perform poorly by rejecting parts from the better board level solderability categories. If the unit has truly good solderability coverage the solderability tests TM2022, MOD2022 and ISTD still may not accept the part, however, if these solderability tests do accept the part then the part will most likely have good solderability coverage.

On the other hand, the parameters F_{spike}, F_{max} and $F_{(2)}$ are shown in Table 10 to be less restrictive and able to reject, for the most part, units which are indeed in the worse categories. Indeed, the parameters F_{spike}, F_{max} and $F_{(2)}$ may not be rigorous enough to effectively screen out units with marginal lead solderability. Nevertheless, the parameter $F_{(2)}$ shows some promise in the ability to discriminate good soldering performance since units which have a force at 2 seconds greater than 100 μN/mm tend to exhibit average or better board level soldering performance while those with $F_{(2)}$ less than 100 μN/mm tend to display average or worse board level soldering performance.

A similar set of data is displayed in Table 11 for the board visual lead categories rather than the board visual score categories. As in Table 10, a similar behavior of the solderability tests is noted. Again we find F_{spike}, F_{max} and $F_{(2)}$ able to distinguish units which are genuinely of poor solderability. That is, these solderability tests rarely pass units with poor coverage. On the other hand, the solderability tests TM2022, MOD2022 and ISTD strive to be able to detect units of good solderability coverage. Unfortunately, this latter group of solderability tests fails too many good units.

Table 10. Solderability Tests Versus Board Visual Score Categories

Solderability Test and Outcome		Board Visual Score Categories A	B	C	D	E
TM2022	Pass	1	0	0	0	0
	Fail	5	6	10	1	0
MOD 2022	Pass	3	4	2	0	0
	Fail	3	2	8	1	0
ISTD	Pass	1	0	1	0	0
	Fail	5	6	10	1	3
F_{spike}	> 300	6	6	7	1	0
	≤ 300	0	0	4	0	5
F_{max}	> 100	6	6	7	1	0
	≤ 100	0	0	4	0	5
$F_{(2)}$	> 100	6	6	5	0	0
	≤ 100	0	0	6	1	3
$F_{(2)}$	> 200	3	3	2	0	0
	≤ 200	3	3	9	1	3

Table 11. Solderability Tests Versus Board Visual Lead-Joint Categories

Solderability Test and Outcome		Board Visual Lead Categories C1	C2	C3	C4	C5
TM2022	Pass	16	2	0	0	0
	Fail	186	99	103	8	0
MOD 2022	Pass	112	46	3	1	0
	Fail	90	55	100	7	0
ISTD	Pass	29	5	1	1	0
	Fail	173	99	117	13	48
F_{spike}	> 300	202	89	61	8	0
	≤ 300	0	15	57	6	84
F_{max}	> 100	202	89	61	8	0
	≤ 100	0	15	57	6	84
$F_{(2)}$	> 100	197	80	27	2	0
	≤ 100	5	24	91	12	48
$F_{(2)}$	> 200	108	33	1	2	0
	≤ 200	94	71	117	12	48

In addition to these results, it is also possible to develop significant multiple regression models that can predict the board solderability score from either wetting balance force parameters or indices. One such model is given by

$$\text{Predicted Score} = 758.76 + 110.16*t_0 + 0.837*F_{max} - 2.143*F_{spike}$$

$$- 2.772*F_{(2)} + 0.00531*F_{(2)}*F_{spike}$$

with an adjusted R-square of 0.89.

This multipie regression model forms a linear combination of the three wetting balance parameters (and their cross products) maximum force attained, wetting force at two seconds and the withdrawal force. It could be used to construct a solderability test by classifying the predicted score of the unit into the appropriate score categories A - E. To the authors' knowledge, this is the first documented, statistically based

relationship between measured, quantifiable wetting properties and board level soldering performance.

Note that this multiple regression model is only valid with respect to 18 lead CERDIP units whose lead finish resembles the finishes contained within this study. Since we have no data on other package styles and lead configurations we may not generalize the applicability of these results to other package styles and lead configurations. However, the regression method is general and may be applied in a wide range of situations with the input of appropriate experimental data.

5. CONCLUSIONS AND RECOMMENDATIONS

This paper has endeavored to explore possible relationships between wetting balance parameters and board level soldering performance and between "dip and look" solderability assessment results and board soldering performance.

Tables 3 through 6 support the conclusion that "dip and look" component lead solderability assessment does have a meaningful association with board level soldering performance. In this study we have seen that solder joints, acceptable to MIL-STD-2000, can be produced using component leads that exhibit some level of asperity pinholes, dewetting and even non-wetting. We have also seen that no statistically significant difference in board level soldering defects were observed between component leads exhibiting 95 - 100% solder coverage and those exhibiting 75 - 94% solder coverage when using acceptance per MIL-STD 2000 as a response variable. However, the component leads exhibiting the 95 - 100% coverage did produce the best distribution of high quality joints. These results also suggest that even with the use of the 95% coverage requirement, some MIL-STD-2000 defective joints may form, (2 out of 126 in this study).

The use of measurable variables data from the wetting balance has shown statistically significant correlations with board level soldering performance in this study. While many wetting balance indices and wetting force parameters exhibited statistically non-zero correlations (Tables 7 and 8), only the wetting balance indices MAXANG and DeVore's coefficient of wetting, CW showed strong correlation (values close to 1 or -1) with the number of holes not filled. This is consistent with the unofficially reported manufacturing experience that "the solderability of the component lead affects the final joint more than the solderability of the board plated through holes."

Through the use of discriminant analysis special "discriminant functions" were generated to classify the board level soldering performance of semiconductor components. In this study 33 out of 36 units were correctly categorized using this

technique. Although these particular discriminant functions may not apply outside the given process for which they were developed, the method of using discriminant analysis may offer some promise for classification of visual board level soldering performance results on the basis of wetting balance data.

Comparisons of various solderability tests with respect to board level soldering performance (Tables 10 - 11) indicates that the current wetting balance based tests may be overly critical by rejecting units that would otherwise produce acceptable solder joints per MIL-STD- 2000. The use of other wetting balance parameters such as F_{spike}, $F_{(2)}$ and F_{max} as a criteria for component solderability assessment show good agreement with board level soldering performance with respect to MIL-STD-2000 acceptable and grossly rejectable solder joints. Nevertheless, these wetting balance parameters are not as effective at screening out marginal component leads that produce MIL-STD-2000 rejectable solder joints. These data indicate that a reasonable "critical value" of $F_{(2)}$ is between 100 and 200 μN/mm.

A statistically based multiple regression model has been formulated which predicts board level soldering performance using information from the wetting parameters t_0, F_{spike}, $F_{(2)}$, F_{max}. This model accounts for 89% of the variability associated with these data.

The results of using wetting balance parameters in statistically derived models or discriminant analysis seem encouraging as methods for predicting or classifying board level soldering performance.

The results of this first study indicate that both " dip and look " visual assessment of component solderability and wetting balance parameter measurement of component solderability assessment have meaningful and statistically significant associations with board level soldering performance. However, from this data set there is no clear choice as to which assessment technique is superior. The wetting balance does offer the advantage of providing variables data on solderability assessment, and a formula for predicting board level soldering performance based on wetting balance parameters has been developed which does not exist for visual inspection results.In direct one-to-one comparisons[6,7] of visual " dip and look " component solderability assessment with wetting balance parameter/indices assessment, no correlation above 90% was achieved. It is the authors opinion that higher correlation than 90% may not be possible.

As suggestions for future work, perhaps a more objective measure of percent coverage would lead to a more precise statement of the relationship between wetting balance parameters and board level soldering performance. If the discriminant method is applied to various package types it would be instructive to see how the

discriminant functions change. Although both the "dip and look" and wetting balance approaches seem to be correlated with board level soldering performance, the authors believe that further refinement of the wetting balance technique offers improvement opportunities over the unpredictable variability of the "dip and look" method.

APPENDIX: COMPENDIUM OF WETTING BALANCE TESTS AND INDICES

Devore's Solderability Index

John DeVore[3] proposed a solderability index, here called SI, defined as

$$SI = \frac{F_{(2)}}{t_0 (F_{spike} - F_{end})}$$

It is worth noting that SI is invariant with respect to the perimeter soldered and is unique among other proposed indices in that it incorporates values relating to wetting speed (t_0), wetting force ($F_{(2)}$) and dewetting ($F_{spike} - F_{end}$).
In addition, DeVore has recommended that "good" solderability is achieved when SI exceeds five. Thus an informal solderability test could consider a unit passing whenever it achieves a value of SI exceeding five.

Devore's Coefficient of Wetting

DeVore[2] has also discussed a measure called the coefficient of wetting, here defined as

$$CW = \frac{F_{eq}}{t_{eq}}$$

The sample must reach equilibrium in order for this index to be calculated. In practice, this may be overly restrictive for many units do not attain equilibrium with the usual five second wetting balance test. Moreover, experience with computing this index demonstrates that there may be some difficulty deciding exactly when the equilibrium point has been reached.

Stability of Wetting Index

Becker[2] alludes to a stability of wetting measure which we call SW and define as $SW = F_{max} - F_{end}$. Note that this index is primarily concerned with dewetting.

Industry Standard Solderability Test

Becker[1] mentions an informal industry standard solderability test which defines a unit to pass if $F_{(2)} \geq 300\ \mu N/mm$. The essential variable of this test is $F_{(2)}$, the wetting force obtained after two seconds have elapsed since the initial immersion of the termination into solder.

MIL-STD-883/TM2022 Solderability Test

This method considers a unit to pass during a 5 second test if $t_0 \leq 0.59$ seconds and $F_{(1)} \geq 2/3\ F_{(5)}$. The principle variables are the initial recovery time or time to zero force, t_0, which should be less than or equal to 0.59 and the time to achieve two-thirds of the maximum force exhibited during the test, $t_{2/3}$, which must be less than or equal to one second.

Wooldridge's Modified MIL-STD-883/TM2022

Wooldridge[11] describes a modification of the MIL-STD-883/TM2022 test whereby a unit is considered to pass the test if the following three conditions are satisfied, $t_0 \leq 1$ s, $F_{(2.5)} \geq 200\ \mu N/mm$ and $F_{(5)} \geq 200\ \mu N/mm$.

The essential parameters for this test are t_0, the time to recross the zero force line, $F_{(2.5)}$, the force at 2.5 seconds and $F_{(5)}$, the force at 5 seconds.

Percent of Theoretical Maximum Force

The theoretical maximum wetting force, F_{th}, can be defined as the surface energy or surface tension of the solder at the temperature of interest. Manko[5] has published 490 dyne/cm @ 280 C for 63/37 solder. Some of the industry experts have informally agreed at the recent EIA and IPC meetings that the value should be closer to 420 dyne/cm = 420 $\mu N/mm$. We have chosen to use Manko's published value of 490 $\mu N/mm$ in this paper. With this value we may now define the percent

of the theoretical maximum wetting force as

$$PCTF_{th} = 100\% \frac{F_{max}}{F_{th}}$$

This index, like DeVore's SI, is invariant with respect to perimeter.

Angle to Maximum

Mullenix, Gerke and Kwoka[6] proposed that a useful measure of wetting is the angle formed between the time axis and the line connecting the point of maximum wetting force with the origin (see Figure 4). This may be written as,

$$MAXANG = \tan^{-1}\left(\frac{F_{max}}{F_{th}}\right).$$

Note that MAXANG is similar to DeVore's coefficient of wetting, CW, except that the time and force at maximum (before extraction from solder) is used instead of at equilibrium. This makes the index capable of being computed in cases where equilibrium is not achieved.

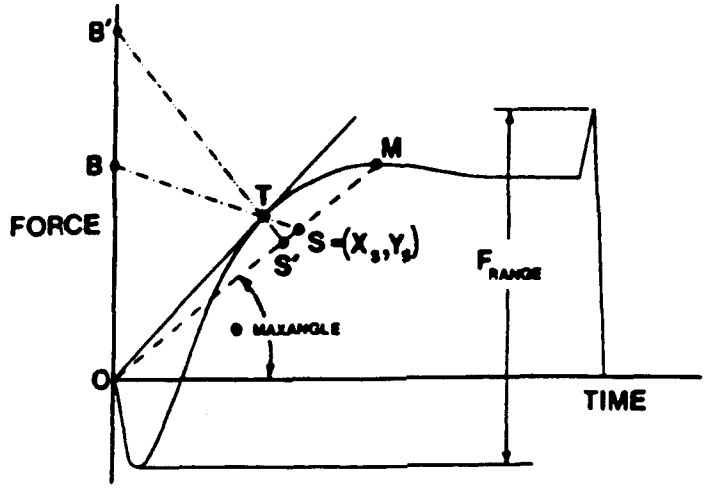

FIGURE 4. Points used to calculate new solderability indices.

Adjusted F_{max}

Point B on Figure 4 displays the idealized "best case" wetting balance curve for a given maximum attained wetting force. Such a curve would rise nearly straight up to a given observed maximum point B then remain at that level for the entire test. In practice a curve cannot follow this idealized curve exactly, but it can approach it by rising steeply, attaining its maximum at point M and leveling off at that maximum value. The adjusted F_{max} proposed by the present authors (Mullenix, [6]) seeks to take the shape of the curve into account and weight F_{max} by how close the shape of the curve resembles the idealized "best case" curve.

To accomplish this, the closest point on the graph to B (see Figure 4) is found by rotating a ray laying on the force axis with tail at the origin, O, toward the time axis. The first point on the curve which this ray meets will be the tangent point, T, formed by the ray and the wetting balance curve. The line segment joining B and T will intersect the line segment $\overline{OM}$ at the point S.

Observe that the steeper the curve rises, the larger the segment $\overline{ST}$ becomes. The ratio $\overline{ST}/\overline{SB}$ gives the proportion of the distance to the "best case" point B accounted for by the location of the point S. The proposed adjusted F_{max}, denoted $ADJF_{max}$, may now be defined as

$$ADJF_{max} = \frac{\overline{ST}}{\overline{SB}} F_{max}$$

where

$$\overline{ST} = \sqrt{(t_{tan} - x_s)^2 + (F_{tan} - y_s)^2}$$

$$\overline{SB} = \sqrt{x_s^2 + (F_{max} - y_s)^2}$$

and (x_s, y_s) are the coordinates of the point S with

$$x_s = \frac{t_{tan}}{1 + \frac{t_{tan}}{t_{max}} - \frac{F_{tan}}{F_{max}}}$$

$$y_s = \frac{F_{max}}{t_{max}} x_s .$$

Adjusted F_{th}

The present authors[6] proposed an adjustment to F_{th} similar to the construction of $ADJF_{max}$. Using line segments from Figure 4 we define

$$ADJF_{th} = \frac{S'T}{S'B'} F_{th} .$$

Figure 4 shows the line segments in the above formula and in particular displays the point B' on the force axis which is equal to F_{th}. With the substitution of F_{th} for F_{max} in the formula for x_s given above in the computation of $ADJF_{max}$, the same formulae may be used to compute the coordinates of the point S'.

Force Range

The force range, also proposed by the authors[6], is simply $F_{range} = F_{spike} - F_{min}$. As with the stability of wetting index, SW, the force range is mainly intended to assess the effects of dewetting.

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Mark became a Certified Electroplater-Finisher (CEF) in 1983. He was issued his first U.S. Government patent for matte tin reflow processing in 1987. He was issued his second patent in 1989 for leadless chip carrier soldering. Mark has published and presented four technical papers on soldering and solderability testing and has led an IPC seminar/workshop discussion group on solderability testing.

Mark holds a BS degree in Chemistry from the University of South Florida and a master's degree in Chemical Engineering from Purdue. He is a member of the American Electroplaters Society, ACS, and AICHE. He is also Chairman of the EIA Soldering Technology Committee and Co-Chairman of the Joint IPC/EIA Task Group drafting the ANSI/J-STD-002 Solderability Test Method. He is a member of the Steam Age/Solderability Task Group, the IPC Accelerated Aging Task Group, and the IPC Wetting Balance Task Group.

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TECHNICAL BREAKTHROUGH - LIGHTING FOR FINE PITCH INSPECTION

by

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Abstract

Many attempts have been made to develop Automated Optical Inspection Systems for the inspection of circuit assemblies. Most have suffered from an inability to reliably detect defects with an acceptable number of false alarms. However, recent advancements in lighting and inspection methodologies have found wider acceptance of this technology by the manufacturing community.

This paper contains a brief history of the automated optical inspection of printed circuit boards. A summary of the various methods which have been attempted and an analysis of the strengths and weaknesses of each inspection technique is discussed.

The body of the paper presents an in-depth discussion of the tools and techniques employed in the latest generation of equipment from Control Automation, highlighting especially the proprietary patented lighting fixture.

LIGHTING FOR FINE PITCH INSPECTION

BACKGROUND

During the 1980s when large numbers of machine vision companies were being formed, many companies attempted to create inspection systems for populated printed circuit boards. These ranged from relatively simple products such as the original Interscan 1500 which inspected pin through-hole, to complex systems which inspected the top of PCBs for component presence/absence, polarity, and part number.

It quickly became apparent that only systems which inspected for a relatively narrow set of circumstances, such as pin through-hole only, had any hope of actually working in a manufacturing environment. Machine vision was at that time, and in fact still is today, incapable of handling large number of variations in what constitutes a good assembly.

The original Interscan products from Control Automation utilized 4 angled cameras placed 90 degrees apart and angled 30 degrees to the perpendicular. The lighting consisted of a combination of LEDs and fluorescent bulbs. The entire inspection methodology consisted of creating a glint off the angled lead which was reflected into one of the four cameras (See APPENDIX A - figure 1).

Other products utilized such exotic techniques as galvanometer driven mirrors which reflected the field of view into the camera, systems utilizing varieties of shutters and fiber optic bundles to view the PCB from several different directions, and systems utilizing single or banks of vertical cameras and strobe lights, just to name a few.

Then there were the processing intensive systems which were variants on the technique commonly referred to as "Morphology." These systems did not have to rely on clever lighting systems, because they claimed to actually be capable of analyzing the image directly. Later, laser-based systems emerged which utilized a triangulation scheme to create three dimensional images. And most recently, several variants on X-Ray technology have emerged primarily involved in post solder inspection.

The common thread among all the successful entrants into this field is the image. If the image which is created provides sufficient contrast between the defect and the acceptable condition, and the acceptable condition does not have too many variants, then the inspection can be reliably performed. However, arriving at this high contrast image and a means for inspecting it is not a simple matter. Because the object under inspection is invariably a complex image with many competing features and reflective surfaces, very careful attention must be given to the creation of the image and the inspection technique.

CURRENT INSPECTION TECHNIQUES

Let's take the example of a post solder inspection of the metalized end of a 1206 device. If you were to view this surface from directly above, the soldered surface would appear highly reflective under normal ambient light conditions. However, depending on the type of pad the component is placed on, this pad may also be highly reflective in the absence of solder. Although a human might be perfectly capable of differentiating the two conditions under these circumstances, an automated system will invariably have problems.

Now there are a variety of ways to perform an automated inspection of this joint. One is to view the joint from the front - at an angle to the perpendicular, 30 degrees in our case, and illuminate the joint from the sides. The resulting reflections from the meniscus of the solder joint are completely absent in the un-soldered case. This is a high contrast image which can be automatically inspected. See figures 2 and 3 for examples of this. Another technique involves viewing the solder joint from the sides and lighting the joint from the front. Here again, you can see a high contrast image between the soldered and unsoldered case (See figure 4). Which one to use? It depends.

And what it depends on is the pad geometries, the solder process, the component density, screen printed characters, etc.. The short answer is there is no single answer. And this is true for all inspection systems. X-Ray systems suffer from confusion due to internal traces and components mounted on the other side of the board. Laser systems suffer from problems due to extreme reflectivity and retro reflections of the laser beam. So the key here is flexibility in creating the image and a means for inspecting it.

There are several elements to our approach to this problem. One, Control Automation has developed a very flexible lighting and camera arrangement (See figure 5). This hemispherical (elliptical for higher magnifications) lighting fixture utilizes high intensity LEDs at all latitudinal and longitudinal intersection points. This patented arrangement provides individual control of every LED. The software controls the specified lighting mode, and varies the pattern of each camera accordingly.

The other element is the inspection technique and the teaching methodology. The post solder inspection process consists of five window types;

1. Search
2. Presence/Absence
3. Reverse Presence/Absence
4. Void
5. Bridge

The Search Algorithm consists of two 1 dimensional correlations, in X and Y. This algorithm finds the location of the bright feature relative to the trained location of the window. Components with multiple search windows are computed as to the location of the entire component based on the individual locations of the search

windows. The search window has the property of moving all the other windows associated with that component.

The Presence/Absence window computes the distribution of intensities within the window. Windows with a very bright area surrounded by dark areas will exhibit a high reading. Windows containing uniform intensities will exhibit low readings.

The Reverse Presence/Absence window is the same as Presence/Absence except that the reading must not exceed the pass level in order to pass. Essentially, this means that the window is looking for a uniform intensity distribution as the correct case.

The Bridge window looks for horizontal continuity as an error condition. The Void window looks for horizontal discontinuities as an error condition.

TEACHING

These simple tools are the building blocks for all the inspection templates. Creating an inspection template involves the use of the CDES Component Designer package which runs on any IBM PC or compatible. Here, the different inspection windows are combined with the appropriate dimensional information to produce the inspection template for a given component type.

These inspection templates are downloaded to the machine during a Library download process. This is followed by a CAD download process where the coordinates of all the components are specified along with their names and rotation. See figures 6 and 7 for examples of inspection templates superimposed over the components they are designed to inspect.

Notice that the templates contain a large number of window types. The type and number of windows used are totally dependent on the user and the library he chooses. Each window type also has associated with it the cameras used and the lighting mode required. As an example, a bridge window located between two leads would be inspected from the camera facing the two leads with the lighting coming from the front, i.e., from behind the camera (See figure 8).

Another example might be a window inspecting for the lifted lead condition. Here the lead is inspected using a void window. It is inspected from both sides using lighting from behind. The idea here is that a properly placed lead will form a continuous bright connection between the lead and the pad. A lifted lead will cause a break and consequently fail (See figure 9).

PERFORMANCE

Now you might be saying to yourself, "Well all this is very nice, but how do I know it works?" The answer to this is the "Performance" feature.

Performance is a utility where the user characterizes the readings from boards with no defects, to boards with 100% defects. A histogram is generated which depicts the readings from these two populations (See figure 10).

The idea is that defective windows should exhibit lower readings than good windows. And if a board with all defective windows and a board with all good windows are inspected, the resulting population of readings will immediately characterize the effectiveness of the inspection methodology.

If the inspection methodology is good the curves will not intersect, that is, the highest readings from the board with all defects will be lower than the lowest readings from the boards with no defects. The resulting gap specifies the value that the pass level should attain. If the curves overlap, then selecting a pass level will

therefore specify a level of detection of less than 100 % and or a level of false flags greater than 0.

Creating these performance curves involves the inspection of three board types;

1. A good board
2. A populated unsoldered board
3. An unpopulated soldered board.

The system automatically compares the readings from the appropriate boards based on the defect type. For example, if a window type is inspecting for the presence/absence of a solder joint, then the system compares the readings from all of that window type found on the good board to the populated unsoldered board. This insures that the readings are unaffected by the presence of the component, because the components are present in both cases, the only difference is the presence/absence of the solder. Another example might be a window inspecting for the presence/absence of a component. Here, the two boards which would be compared would be the good board to the soldered unpopulated board.

These performance curves are the best way to characterize the inspection process without actually running many boards through the system and then manually inspecting them. This also avoids the constant tweaking which plagued many early automated optical inspection systems.

INSPECTION

All Interscan systems utilize a continuous scanning, random lighting inspection methodology. The head continuously moves over the PCB in horizontal scans indexing to the next scan in a serpentine fashion. The lighting mode for each view is determined by the lighting mode required by the windows within the view. Views containing multiple lighting modes are rescanned until all the combinations have been exhausted.

The images are captured by virtue of the stroboscopic effect of the LEDs. The appropriate LEDs are strobed to create the desired lighting mode at the precise instant when the inspection head is located above the view.

The inspection is broken into three discrete board scans;

1. Warp Scan
2. Search Scan
3. Inspection Scan

The warp scan utilizes a projected cross and a triangulation technique to measure the distance from the board to the cameras. This is critical for inspection, because the board warpage must be known in order that the windows can be located correctly.

The Search scan is functionally identical to an inspection scan, except that only search windows are inspected. After the search scan, all inspection window locations are adjusted prior to the inspection scan (See figures 11 and 12).

SYSTEM UTILITIES

The system includes all the required tools for manual editing of the board program and retrieving or storing board programs to disk or tape. The system supports the operation of a barcode reader, error marker, error printer, and remote host.

A worksheet utility is included which permits the user to see at a glance the distribution of lighting modes and window types. This utility will also provide recommended pass levels for all window types automatically (See figures 13 and 14).

The internal statistical package tracks defects by component and defect type. The off-line statistical package can be flexibly configured to provide graphical analysis of any defect types. This PC based package can perform graphical analysis such as Pareto, Scatter Plots, and C Charts (See figure 15).

SYSTEM DESCRIPTION

All menus are superimposed over the video image on a color monitor. A mouse driven user interface is included which is easy to use and convenient. A set of 4 buttons can be used to operate the system when in production. This mode of operation, called operator confirmation mode, enables an operator to review all failures and either accept or reject them (See figure 16).

The equipment is factory hardened, VME based, production equipment. The only moving part in the system is the XY table which is a 1 mil accuracy table with precision lead screws, ball nuts, and an advanced brushless DC motor drive. The system comes standard with a conveyor for in-line operation.

CONCLUSION

Automated optical inspection of printed circuit assemblies has progressed steadily over the last ten years. The current generation of equipment is gaining acceptance in the marketplace as necessary production equipment.

APPENDIX A - Figures

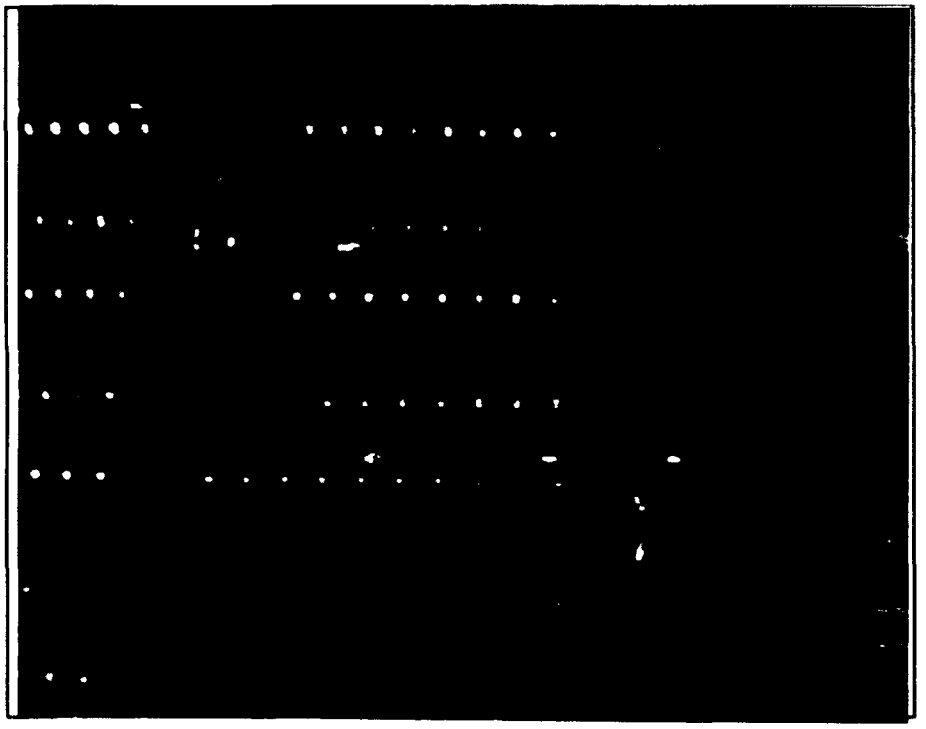

Figure 1

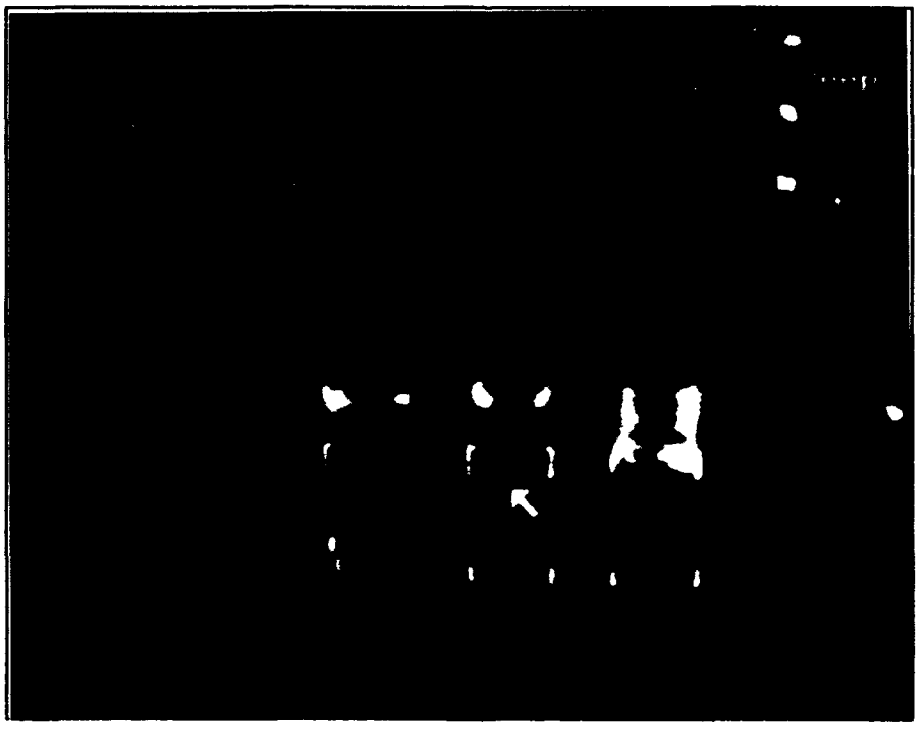

Figure 2

APPENDIX A - Illustrations

Figure 3

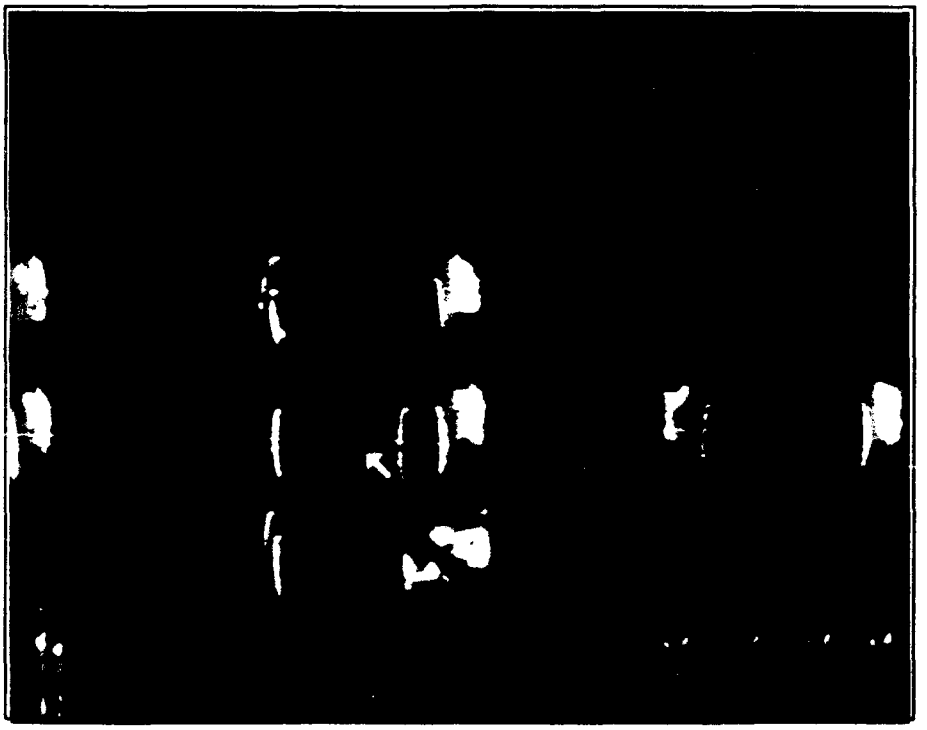

Figure 4

APPENDIX A - Illustrations

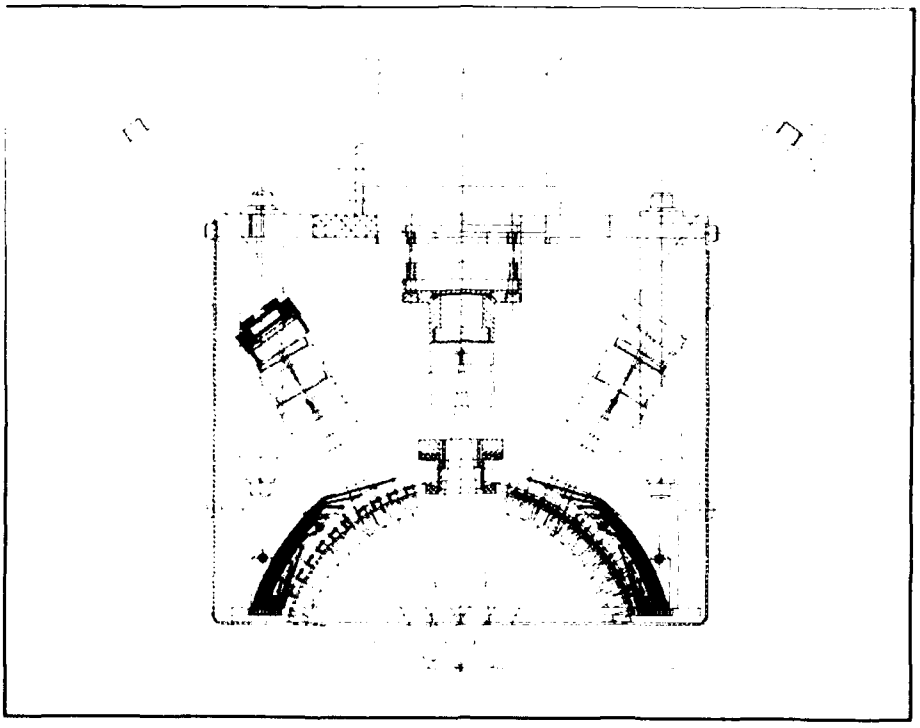

Figure 5

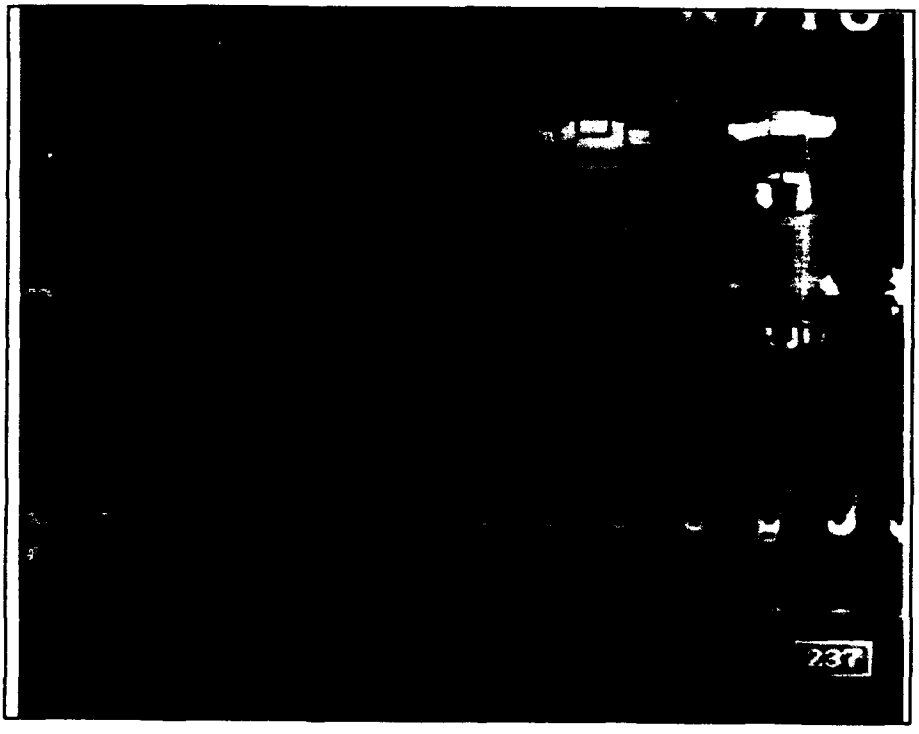

Figure 6

APPENDIX A - Illustrations

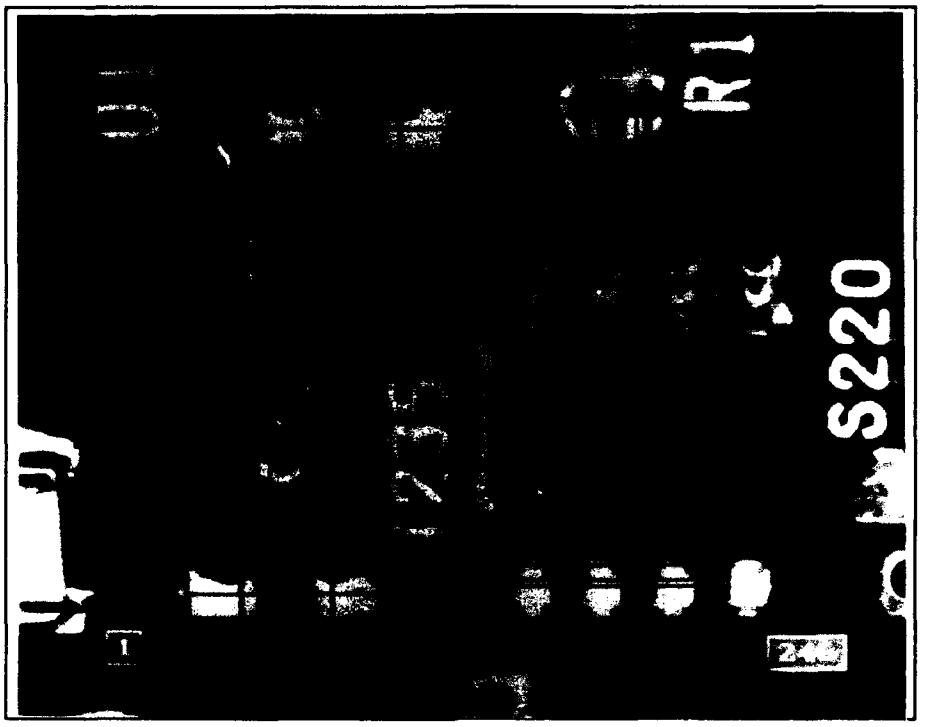

Figure 7

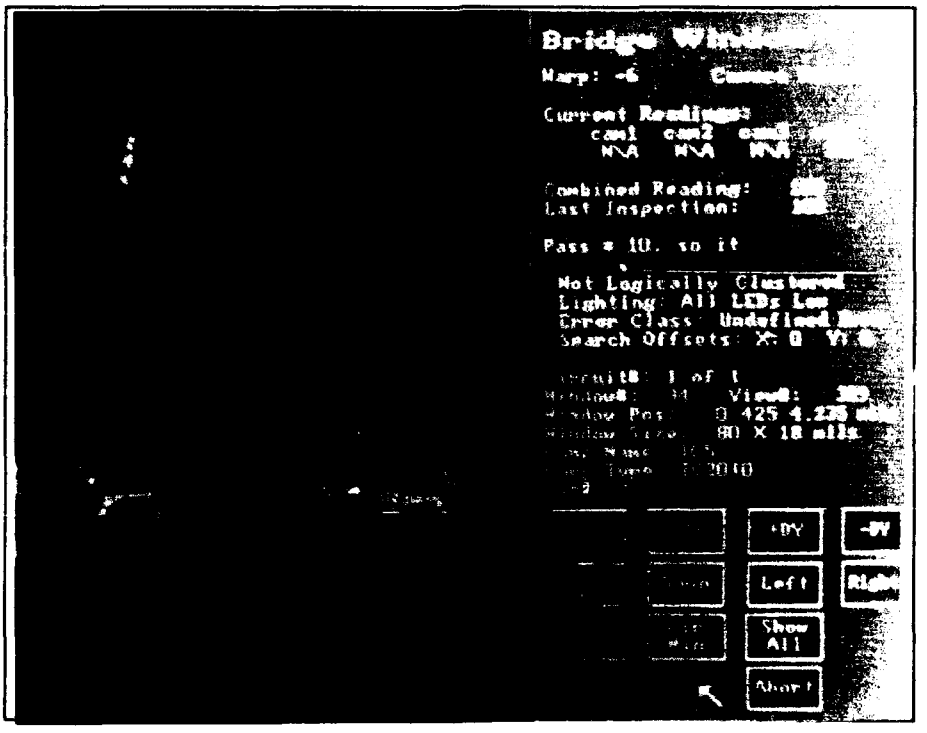

Figure 8

APPENDIX A - Illustrations

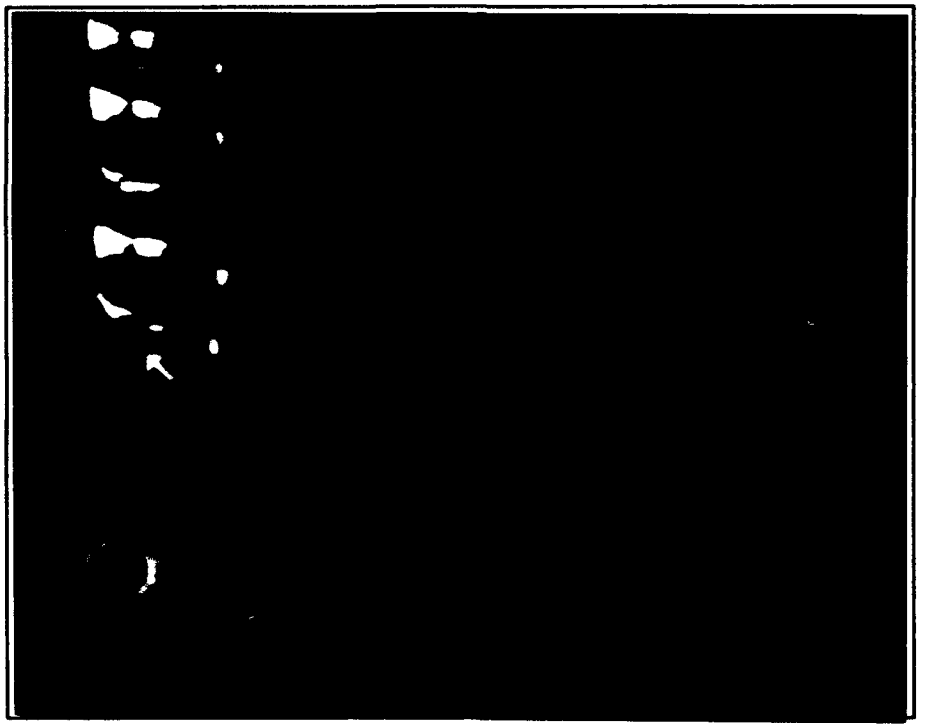

Figure 9

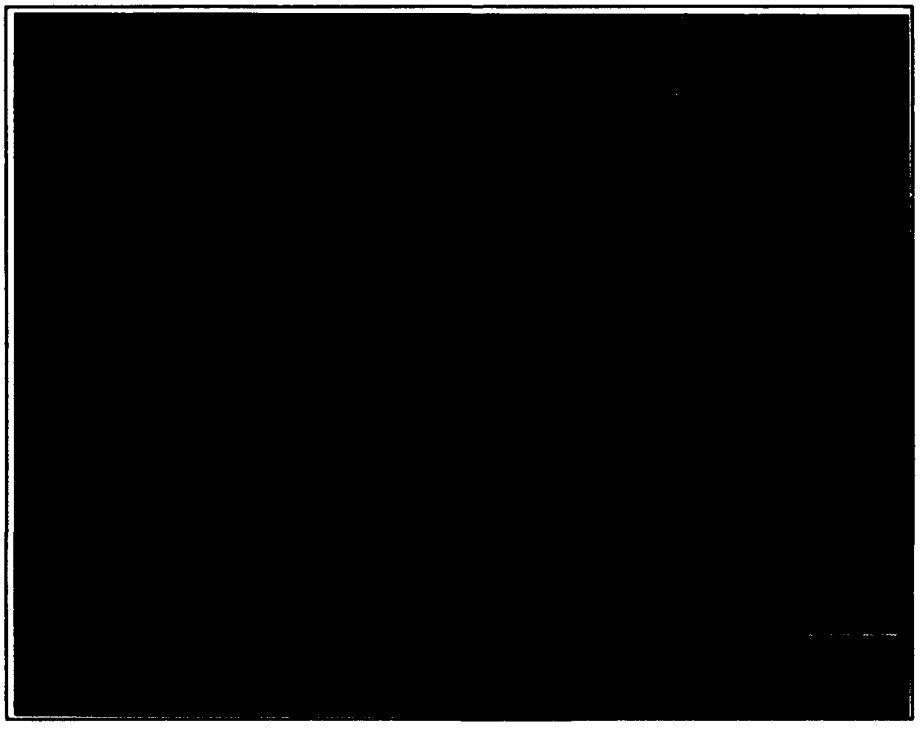

Figure 10

APPENDIX A - Illustrations

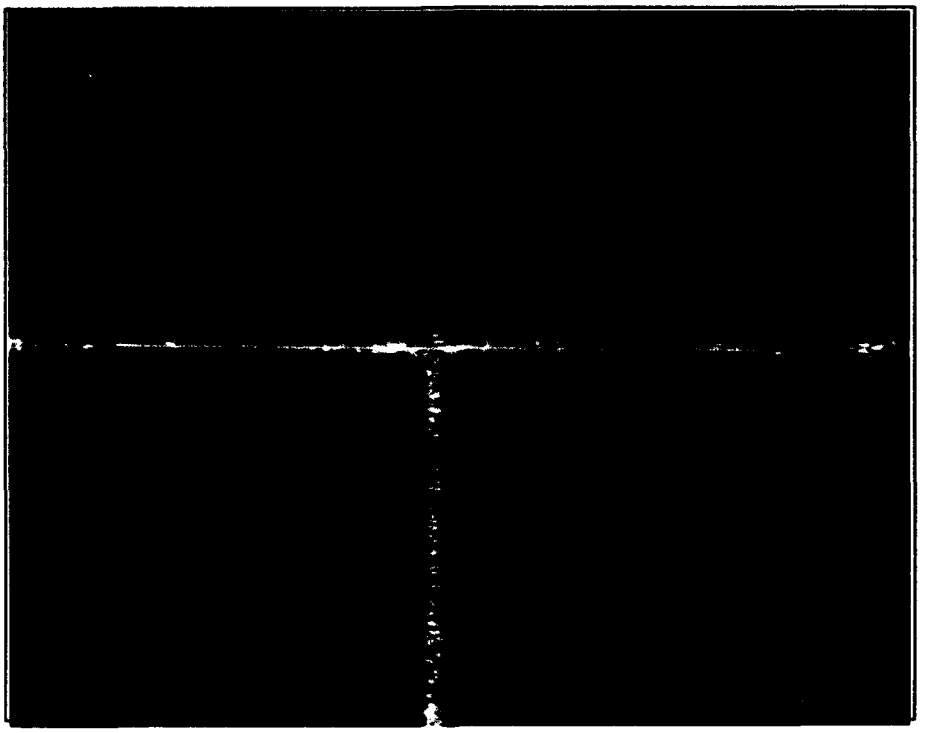

Figure 11

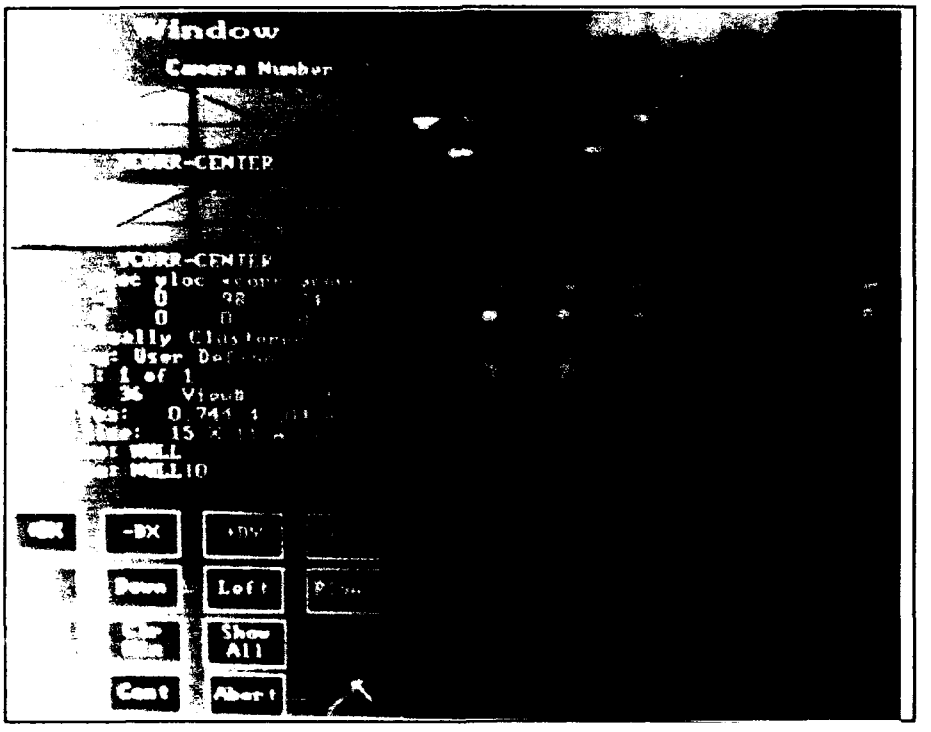

Figure 12

APPENDIX A - Illustrations

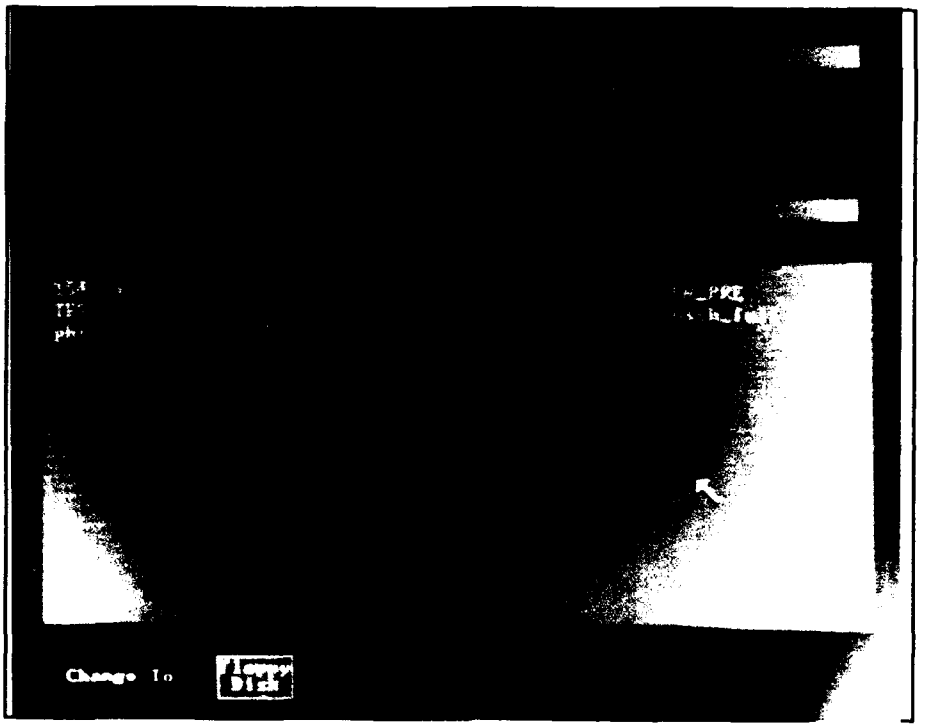

Figure 13

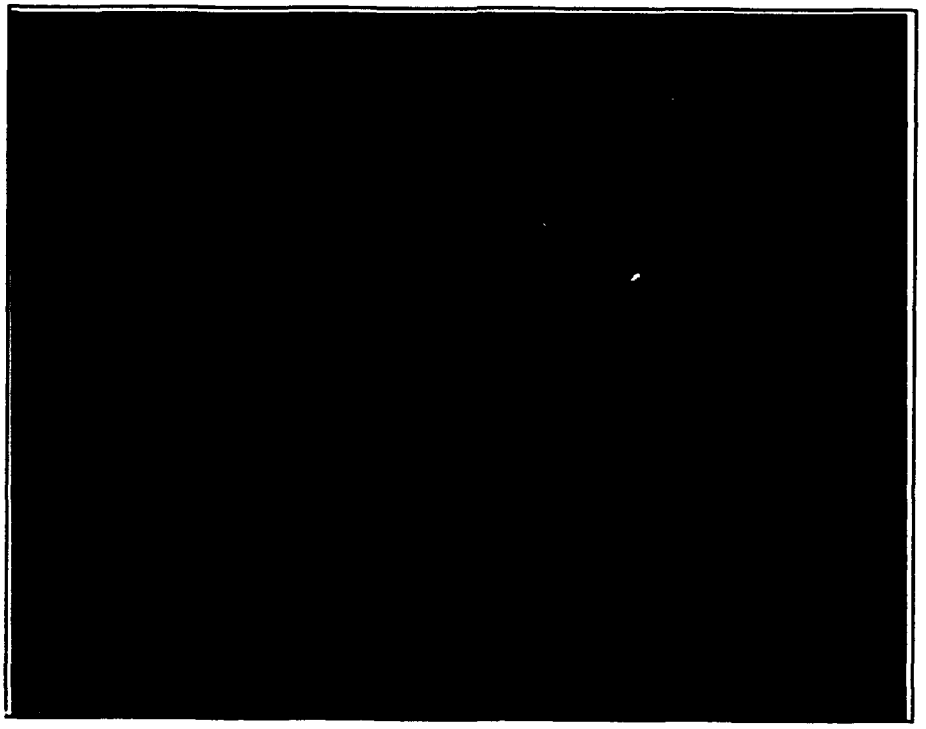

Figure 14

APPENDIX A - Illustrations

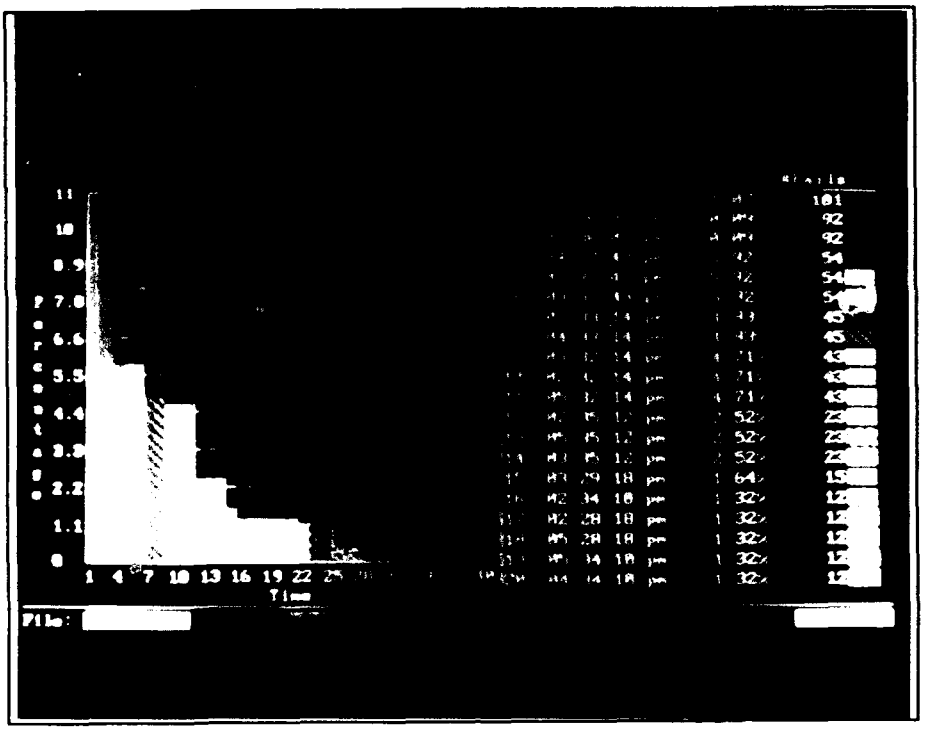

Figure 15

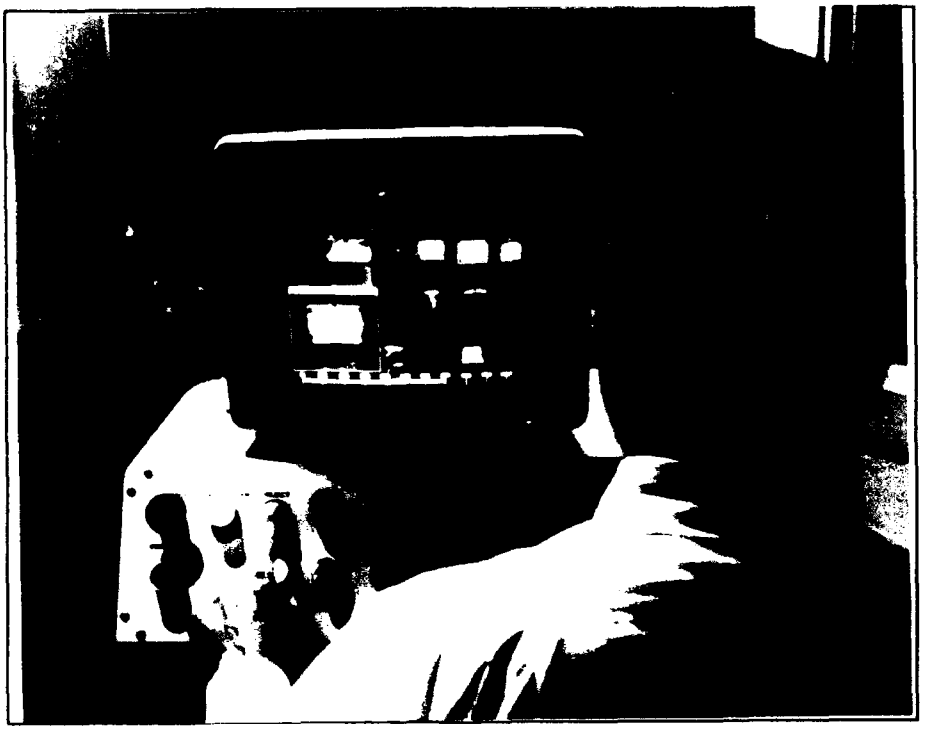

Figure 16

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COMPENSATED SOLDER STENCILS THROUGH ARTWORK MICROMODIFICATION

by

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ABSTRACT

The amount of solder required for adequate solder filleting of surface mount components does not always correlate to the amount of solder deposited during screening or stencilling. The problem arises in the fact that one-to-one artwork of the stencil relative to the printed wiring board provides adequate solder volume for some but not all of the components. One method by which to compensate for this mismatch involves a stencil comprised of two thicknesses. A new approach involves micromodification of artwork from which a single thickness stencil can be made.

MICROMODIFICATION

INTRODUCTION

In common practice, solder stencil artwork is duplicated from top pad artwork of the printed wiring board. This practice usually satisfies the solder requirements of a majority of components and assembly conditions for the respective printed wiring board assembly. However, in our quest for zero defect soldering, this practice, unaltered, has its limitations.

Because of the wide range of surface mount components and their associated tolerances, pad (land) size adjustments, made to accommodate possible supplier differences, will invariably differ amongst component types. This same degree of variation in component dimensions and their associated tolerances also impacts the amount of solder deposit required for a given component type. These required variations, when uncompensated by stencil design, translate into solder defects. It is therefore necessary to modify stencil design in order to eliminate these design induced solder defects. There exist several ways by which to compensate for these design differences. One method is to alter the solder stencil artwork during the origination of the artwork design. Another is to vary the thickness of the stencil itself. Finally, a new technique allows the land artwork to be modified through image alteration. This latter option provides the most flexibility, at the lowest cost.

MICROMODIFICATION TECHNIQUE

The micromodification technique involves photo alteration of image size through precision image modification. By this method, land size can be selectively altered to allow for variation in solder deposition. Land size can be increased or decreased, a variety of times, within the same artwork, for different component types. This technique alters land size without changing circuit layout as land centerlines remain fixed.

The process of micromodification is performed by allowing the next generation artwork to orbit in a clockwise fashion below the original stationary master artwork during exposure to an overhead point light source. A negative original master allows the image to spread to an increased size on the orbiting positive film. A positive original master allows the image to reduce to a smaller size on the orbiting negative film. An identical positive film is subsequently made from the completed negative film.

Land width can be altered from as little a 0.001 in. to as much as 0.200 in. Due to the method of modification, a change in land width is duplicated by a corresponding change in land length (eg. 0.004 in. increase in land width represents an increase of 0.002 in. per side, as measured from the center line of the land.) Also, the method of modification may influence some rounding of land corners, for large alterations. Effective image area can accommodate most board sizes.

APPLICATION

In the fabrication of ceramic copper thick film multilayer interconnect boards, the top surface condition of the boards presents more of a solderability challenge than that found with conventional printed wiring boards. Oftentimes, surface preparation of the metallized lands is necessary in order to promote good solderability. Even so, solderability of the land's perimeter still presents a unique challenge. The top surface of the ceramic board is comprised of a combination of metallized footprints and dielectric layers.

The land perimeter interface of glass and copper is a region of transition in which glass and copper can intermix and whose boundary and topology is somewhat difficult to hold with good line definition. The glass and copper intermix boundary does not promote as good solderability as the rest of the land surface. The topology at this boundary may offer a less than desirable surface for solder paste deposition. Lastly, a one to one deposit of solder paste onto the land may not adequately cover the land perimeter due to process tolerances of both solder paste deposition and board fabrication. It has been found that overprinting of solder paste beyond the land's edge overcomes these process deficiencies, promoting good solderability inclusive of the land's perimeter.

It has been found that an increase of 0.006 in. provides adequate coverage without compromising other assembly attributes. In the case of fine pitch (0.025 in. or less), a minimum gap must be maintained, in order to prevent solder bridging. For our particular process, a minimum gap of 0.008 in. is preferred. This in turn requires that 0.025 in. pitch components be limited to an overall increase in land dimension of 0.004 in. This provides a 0.002 in. increase per side, as measured from the centerline of the land.

As detailed earlier, micromodification can also be used to compensate for specific component styles which require more or less solder than the normal population. In this way, a solder stencil and its associated artwork can be devised to complement the majority of component types, with the fallout addressed through micromodification. The current application involves both standard pitch (0.050 in. spacing) and fine pitch (0.025 in. spacing) leadless chip carriers as well as chip resistors and chip capacitors.

An existing master artwork is micromodified 0.004 in. for the fine pitch components and 0.006 in. for the balance of components (standard leadless chip carriers and passive chip components), with chip capacitors as the only exception. The majority of chip capacitors (including tantallum capacitors) have a wide tolerance of physical dimensions. Land dimensions are typically oversized to compensate for this variation. They further have the largest terminations due to their overall termination size and component height. These components typically require additional solder beyond that of the normal population of components. This style of component requires that the solder deposit extend an additional 0.020 in. beyond the normal addition of 0.006 in. for a total increase of 0.026 in. (0.013 in. per side). For these larger extensions, adjacent land spacing must be checked to ensure a minimum of 0.008 in. clearance. Should the minimum clearance be jeopardized, a smaller increase in land extension should be selected. Chip resistors and very small chip capacitors lack the size and variation to require this additional extension and in fact, additional extension would translate into additional solder defects.

Prior to micromodification, the process had been modified to minimize these types of defects. To increase solder paste spread, multiple screen printing passes were made. These additional passes added to the solder paste volume and mechanically increased the solder paste spread. This approach increased the variability of solder deposit and increased the likelihood of solder bridging. As such, it diminished process control and increased solder defects. The method by which selective chip capacitors received additional solder paste involved selective blocking of a second screen, leaving open only those areas requiring additional solder.

A second printing using this specially modified screen was made, following the multiple first pass printing required for additional solder spread. This process involved multiple screenings, multiple setups, multiple screens, and special screen modification through screen blocking. Through micromodification, this process was replaced with a single screen and single printing. This is in turn resulted in improved process control and ultimately fewer solder defects.

For the cost of artwork micromodification, two screen printings were eliminated, a need for a specially modified second screen was eliminated, solder bridging was corrected, and overall solder defects were reduced. The cost of this micromodification was significantly less than the cost which would be associated with modifying the artwork through the engineering data base.

SUMMARY AND CONCLUSIONS

Micromodification offers manufacturing an economical method by which to alter artwork without involving significantly increased engineering cost. Through micromodification, the soldering process can be easily adjusted to variations in both materials and processes.

ACKNOWLEDGMENTS

I wish to express my thanks to Mr. Arthur Dobie of Microcircuit Engineering Corporation for his assistance in providing me with a technical understanding of the micromodification process of photo image alteration.

James Criscione is an Advanced Manufacturing Engineer at Raytheon. He has had 15 years of experience in electronics assembly, with areas of expertise in surface mount assembly, hybrids, and related materials and processes. He holds a BS degree in Chemical Engineering, as well as an MBA degree, and is the author of several papers.

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COMPLIANT "S" LEAD IMPROVED LCCC SOLDER JOINT RELIABILITY - A CASE STUDY

by

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ABSTRACT

This paper presents an overview of research conducted at Government Systems, Control Data Corporation, on compliant "S" leads for attachment to Leadless Ceramic Chip Carriers (LCCC) and Multichip Modules (MCM). The "S" lead significantly improved the solder joint reliability of the military Circuit Card Assemblies (CCA) studied.

Control Data has been researching the design and manufacture of surface mount assemblies for the past eight years. Since 1987, several design options to improve reliability of LCCC solder joints have been evaluated. The "S" lead for LCCCs has been developed, fabricated and tested, the production processes to assemble "S" leads to CCAs have been developed, and several hundred military Airborne computers using millions of "S" leads have been manufactured and shipped. Control Data has patented the "S" lead technology. During 1990, Control Data developed an improved plated "S" lead.

The completed assemblies are the direct results of Control Data's Advanced Packaging/Processes Research and Development. This paper provides general discussion of the design for manufacturability and manufacturing processes for surface mount assemblies using "S" leads. Although Control Data conducted these research activities primarily to improve reliability of military CCAs, this technology can be used for any commercial application requiring high reliability.

INTRODUCTION

Surface Mount Technology (SMT) with Leadless Ceramic Chip Carriers (LCCC) has taken the lead in commercial electronics as the most successful approach to achieving higher performance, lighter, smaller and less expensive Circuit Card Assemblies (CCA). However, when the successful LCCC technology was applied to military electronics, where the CCA's are subjected to several cycle variations in a thermal environment, solder joint cracks were experienced after relatively few (100 or less) thermal cycles of -55°C to +100°C. The stresses producing these cracks originate primarily from a Thermal Coefficient of Expansion (TCE) mismatch between the component package material and the Printed Wiring Board (PWB) material.

During 1987, Control Data conducted extensive research to improve reliability of the LCCC solder joint and developed the compliant "S" lead and attachment process. The extent to which the manufacturing process design influenced the lead design, the material and process variables that influence solder joint

reliability, and the modifications to the standard LCCC soldering process were addressed during this study. The test program was designed to verify not only the product design reliability, but to demonstrate the process capability to repeatably produce reliable hardware.

Since 1987, several hundred military airborne computers using "S" lead were manufactured and shipped. Control Data has been providing the "S" leads to military and commercial high reliability electronic hardware manufacturers to alleviate the LCCC solder joint reliability problem. During 1990, Control Data developed a plated version of the "S" lead.

BACKGROUND

Control Data incorporated product improvements via tecchnology insertion to the AN/AYK-14(V), the standard computer for Navy Avionics Application during 1986. A module representative of the Preplanned Product Improvement (P^3I) hardware, shown in Figure 1, consists of 6 x 9 inch ten layer polyimide/epoxy glass PWB's densely populated with 0.050 inch pitch 20, 28 and 32 pin LCCC's and fine-pitch gull wing VLSI carriers. A heat sink is mounted either between two CCA's or on just one side of a single CCA.

During early design verification testing, which included thermal cycling and vibration, incidents of LCCC solder joint cracking began to occur. An extensive test program [1,2,3,4,7] was conducted at Control Data to study the factors that determine solder joint thermal fatigue life for a given LCCC/PWB design. Three stages of LCCC solder joint degradation, caused by repeated cyclic strains induced by thermal expansion mismatch are shown in Figure 2-A, 2-B and 2-C. These three stages, visible at 55X or greater magnification with adequate illumination, are 1) stress mark, 2) stress crack and 3) electrically open crack. Numerous solder joints having various stages of degradation after thermal cycling have been cross sectioned. All cross sections revealed a coarse microstructure at the crack tip with Pb-Rich and Sn-Rich phases. The failure mechanism of the LCCC solder joint is covered in detail in reference 1 and 2.

Since the LCCC solder joint failure was a thermal fatigue type phenomenon subject to heavy influence by both product and process design factors, a technical, multi-disciplined task force [5] was formed to reevaluate the product and process design and determine a cost effective solution consistent with several constraints summarized below.

The design constraints were: 1) no impact on the electrical performance of the existing product design; 2) the existing PWB's and the components must be used; and 3) maximum allowable component height increase was 0.075 inch and the maximum junction temperature was 110^{0}.

The process constraints were: 1) to minimize schedule risk and cost, existing surface mount equipments must be used; 2) the solution must be applicable to all products in current production, including nine types (18-68 pin) of 0.050 inch pitch and one type of .040 inch pitch LCCC's; 3) standard rework/repair processes must be applicable, and 4) the CCA's must meet the requirements of WS 6536.

The reliability constraints were: First, test modules designed to include the traditional leaded and leadless components as a control base and the "new" component attachment configuration must pass environmental tests - (1000) thermal cycles over a range of -54^{0}C to $+100^{0}$C with a 1.5 hour cycle time and 20 minutes dwell time at each limit and (750) hours of temperature cycling combined with sine and random vibration patterns to simulate typical avionics vibration requirements; and second, a complete computer system must be subjected to and successfully perform (1000) hours of temperature cycling.

TECHNICAL APPROACH

Based on the results of the preliminary study [1,2] and the industry survey, Control Data decided to examine the following approaches: 1) provide a strain accommodating interface for interconnecting LCCC's to PWB's; 2) use higher fatigue strength joining materials; and 3) minimize TCE mismatch between the LCCC and PWB. These could only be explored in view of the design and process constraints.

After evaluating various factors affecting the thermal life of LCCC solder joint (voids, grain size, fillet size, TCE mismatch), the task force determined [3,4,5,6] that a leaded interface between the LCCC and the PWB represented the packaging design approach that could be implemented in manufacturing within a relatively short time to provide a reliability level acceptable for military avionics. The various types of lead/LCCC interfaces evaluated are shown in Figure 3. The symmetrical "S" shaped compliant lead was selected as the optimal solution. The decision was based on a manufacturability assessment [4] as well as finite element analysis.

The Compliant "S" Lead

The profile of the compliant "S" lead invented[8] during 1987 is shown in Figure 4. The lead material alloy, C17410 (Be .3%, Co .5%, Bal Cu) was selected for high thermal conductivity as well as formability. The raw material is received on reels and the strip is stamped through a series of progressive dies to produce a tie bar that holds multiple "S" leads together on a 0.050 inch pitch. Tooling holes are punched in the bar on a 0.050 inch pitch to facilitate the LCCC/lead attachment process. The "S" lead adds a maximum of 0.070 inch to the component package height. The lead is plated with Sn63:Pb37 solder and a Sn63:Pb37 solder bead is swaged into the tangs of each lead.

Selection of Solder Alloy

The task force evaluated various solder alloys for the "S" lead: Sn63:Pb37; Sn96.5:Ag3.5; Sn99:Sb1; Sn95:Sb5; Sn10:Pb90; Sn50:Pb50; Sn95:Pb5; and Sn97:Pb3. The selection of Sn63:Pb37 was based on the following:

1. Non-eutectic solder alloys have a solidification range of temperature instead of a point, and thus a potential for producing disturbed solder joints requiring rework.

2. The Sn63:Pb37 eutectic solder allows a minimum optimum reflow temperature, which minimizes effects of heating on the parts to be joined.

3. Visual inspection results are relatively well defined for the "bright, shiny" Sn63:Pb37 eutectic solder joint, while this is not true for high tin or lead alloys.

4. Use of several alloys may require different fluxes and cleaners which increases the number of process variables needing control.

5. The metallurgical phenomena associated with the reaction between eutectic solder and common part materials are well understood.

PWB Pad Pattern

The "S" lead was designed to be used with any PWB pad pattern designed for LCCC's[9,10]. However, the task force defined a slightly wider pad pattern to enhance manufacturability. Figure 5 shows the PWB pad pattern design guideline for a 20 pin LCCC.

"S" Lead Attachment Process

The process is outlined in Figure 6. "S" lead strips are cut to length at the tie bar as required, e.g., a 20-pin square LCCC requires four strips of five leads. The strips are mounted on a soldering fixture to produce a lead foot pattern which resembles the PWB pad pattern used for LCCC's, RMA flux is applied and the LCCC's are mounted on the "S" leads. The LCCC/leads are then re-flowed using the vapor phase soldering (VPS) process. The RMS flux holds the LCCC in position relative to the leads before soldering, and the LCCC self-aligns to the leads during soldering because of the surface tension of the molten solder. The solder in the slug on the lead and the solder on the LCCC pad from the tinning operation combine to form fillets around the joint. The tie bar is trimmed after soldering. Figure 7 shows a 20 pin LCCC with "S" leads installed; Figure 8 shows a cross section of the lead and lead-to-component solder joint.

Circuit Card Assembly

The CCA process is outlined in Figure 9. The solder paste (Sn63:Pb37 with RMA flux) is applied to the PWB using a semiautomatic printing machine equipped with two squeegees[9,10] made out of hard rubber. The LCCC's with "S" leads components are then picked and placed on the PWB pads using a robotic work cell. The PWB's are dried at 150°F for 15 minutes to evaporate the volatile solvents in the solder paste and reflowed using the VPS process. Because of the surface tension of the molten solder, the LCCC experiences some realignment to the leads while the leads align to the PWB pads during this second reflow operation. The assembly is cleaned in an in-line cleaning system using freon TMS to remove flux residue. Finally, the assembly is conformal coated in an in-line conformal coating system.

EXPERIMENTAL STUDIES

To optimize the assembly and soldering process parameters, the task force conducted several experimental studies[5,6]. Some of these are briefly described in the following paragraphs.

Solder Plating - After extensive study, it was decided to underplate the leads with 20-30 micro inches of copper prior to solder plating. This copper underplating preconditions the lead surface, and results in a good, reliable metallurgical bond between the base material of the "S" lead and the the PWB and component mounting pads.

Solder Paste Thickness on the PWB - Several circuit card assemblies (CCA's) were built using 0.004 and 0.006 inch thick solder paste and LCCC's with "S" leads. The assemblies were inspected for lead/PWB fillet and solder in the lower 'S' bend. Solder paste, 0.006 inch thick, produced excellent lead/PWB solder joints without significant touch-up/rework. The alignment of the leads was excellent. Solder paste, 0.004 inch thick, required relatively more touch-up/rework at the CCA level. Although

0.006 inch thick solder paste deposited more solder in the lower "S" lead bend, no adverse effect was observed on the compliant lead strain relief performance and solder joint integrity during environmental testing.

Reflow Effects on LCCC/Solder Joints - The LCCC/lead solder joint is subjected to at least two reflow cycles for assembly. Additional reflow could be experienced if rework is required. The multiple reflows of the solder may be of concern because of the possibility of degradation of the solder joint due to the formation of intermetallics and the possibility of microstructural coarsening. An experiment was designed to evaluate the effects of multiple reflowing on the LCCC/lead solder joints. The sets of samples were subjected to 1, 2, 3, 4, 8 and 12 VPS reflow cycles with and without flux. The results of pull test and CuSn intermetallic thickness studies after multiple reflows of LCCC's with "S" leads are shown in Figure 10. The 90^{0} pull strength of the solder joint is approximately constant up to four reflow cycles. However, after four reflow cycles, the pull strength starts to decrease significantly. Repeated VPS reflows cause progressively thicker formation of CuSn intermetallic at the interface between the "S" lead and the solder joint. Excessive numbers of reflows cause degradation in the pull strength of the joints as excessive thickening of the intermetallic layer occurs. Four reflow cycles are required to double the initial intermetallic layer thickness of 0.0001 inches, which is considered to have a negligible effect on strength (See Figure 10).

Reflow Effects on LCCC/Lead Alignment - Attaching an "S" lead as an interconnection between LCCC's and PWB's is a process in which it obviously is possible to induce some misalignment at either end of this connection. The initial attachment of LCCC's to leads, placement of leaded devices on the PWB, and the reflow operations can easily affect the degree of alignment between lead ends and their respective pad locations. During development of the lead attachment process, lead alignment was monitored to assess the effect of the process variables. The degree of LCCC pad-to-lead alignment was measured as the offset of the lead past the edge of the LCCC pad, when viewing the bottom of the LCCC. If the lead is entirely on the pad, the offset was measured as zero. The data was recorded by LCCC serial number and the lead number. These LCCC's were then soldered on the PWB's using VPS and IR reflow processes. The LCCC's were then cut off the PWB's, using a slow speed diamond saw with the cut occurring midway through the lead. This was done to allow the underside of the LCCC to be exposed so that the alignment measurements could be repeated to assess the effect of the second reflow. Figure 11 shows the LCCC pad-to-lead alignment after lead attachment and after soldering the same components on a PWB using both the VPS and IR process. Re-flowing causes the leads to shift in a manner having a self-centering tendency and thus improves the average overall alignment. During VPS, the temperature of all solder joints reaches 215^{0}C and the leads and the components move in the molten solder due to surface tension, thus producing the self-centering effect. Leads on the IR-reflowed samples tended to shift less than did those on the VPS samples (it is suspected that this is due to non-uniform heating inherent to the IR process.

Rework Effects - Several LCC's having "S" leads were soldered on CCA's and evaluated to understand the effect of the following rework situations: (1) Replacement of LCCC's with "S" leads using a hot nitrogen reflow system; (2) the effect that reworking the lead/PWB (bottom) solder joint had on the LCCC/lead (top) solder joint; and (3) the effect of attaching jumper wire(s) on the LCCC/lead (top) or lead/PWB (bottom) solder joint. The results of these experiments on rework are:

1. LCCC's with "S" leads can be successfully removed using the same techniques as for LCCC's without leads, i.e., the hot nitrogen reflow process.

2. The lead/PWB (bottom) joint can be reworked using a 15W iron without raising the temperature of the LCCC/lead (top) joint above 80°C. The top joint does not show any signs of degradation when rework is performed on the bottom joint.

3. Up to three (3) jumper wires can be soldered to the LCCC/lead or lead/PWB joints without degrading the solder joint integrity.

TEST PROGRAM

Test modules were designed[5,6,7] that were representative of modules being manufactured at that time and successfully performed in military avionics applications. Two sizes of test modules were included in the test program. One was 6 x 9 inches and the other was 6 x 4 inches. The test program included both single (heat sink on one side of the CCA) and double (CCA's on both sides of the heat sink) modules. Ten-layer PWB's were designed to include a variety of different component types. The design further provided for interconnection of various daisy-chain-wired components to enable continuity monitoring of all solder joints while the assemblies were undergoing environmental testing. The test setup consisted of a logic-based, computer-controlled, automatic system designed to perform periodic continuity checks. The system, developed by CDC, checked the test circuits simultaneously in 100×10^{-9} sec time intervals. Discontinuities that were detected were stored in the test system memory. The test program included the following tests:

1. One thousand (1000) temperature cycles from -54°C to +100°C, 1.5 hours duration with 20 minutes dwell at each extreme.

2. Seven hundred fifty (750) hours of temperature cycles from -54°C to +100°C, combined with random vibration levels of 1.9, 3.7 and 7.7g RMS, eight (8) hours per cycle.

3. Sine vibration at levels of 5g and 10g.

4. Random vibration at levels of 8.5g RMS and 12.7g RMS.

TEST RESULTS

In addition to continuous monitoring, the visual inspection was performed on a regular basis using 20X magnification throughout the environmental tests. The solder joints on the "S" leaded LCCC's exhibited no failures in any of the tests. In contrast, all solder joints of LCCC's attached directly to the PWB failed during thermal cycling [5,6,7]. Also, a complete AN/AYK-14 computer system successfully performed during 1000 hours of operational test with no failures.

FIELD EXPERIENCE

The "S" lead technology was approved by the Navy and Air Force customers in 1987. Control Data has shipped more than 1300 military airborne computers and several hundred modules using more than 25 million 'S' leads to various military programs, and provided the "S" lead technology to several manufacturers of military and commercial equipment. No "S" lead solder joint failures have been reported.

PLATED "S" LEAD

During 1990, Control Data developed an improved "S" lead which significantly enhanced the manufacturability during lead fabrication and assembly processes. Figure 12 shows a plated "S" lead (1990 invention) and an "S" lead with a solder bead (1987 invention). On the plated "S" lead, thicker solder plating was used and essentially replaced the solder bead. The leads are formed first and then plated with 20 to 30 microinches of copper followed by a predetermined amount of Sn63:Pb37 solder plating. This design minimizes the solder build-up in the lead bend after reflow soldering, improves compliancy of the lead, and reduces rework. The test modules assembled using these leads have completed thermal cycles equivalent to approximately 15 years in an avionics field environment, and the AN/AYK-14 VHSIC (the latest technology insertion) computers have nearly completed the required qualification testing without any "S" lead solder joint failures. A patent aplication for this lead has been filed.

"S" LEAD FOR MCM

Control Data has developed an application of "S" leads which attaches MCM's to a motherboard as shown in Figure 13. This design concept not only protects fragile wire bonded or Tape Automated Bonded (TAB) chips on the MCM's but facilitates the attachment of a heat sink on the exposed substrate surface to transfer heat via convection. The leads can be attached by vapor phase or manual soldering process.

CONCLUSION

1. An S-shaped Cu/Co/Be alloy lead will accommodate the strain between surface mounted LCCC's and PWB's that occurs in cyclic thermal environments.

2. The plated "S" lead has significantly enhanced the manufacturability of lead fabrication and lead assembly processes.

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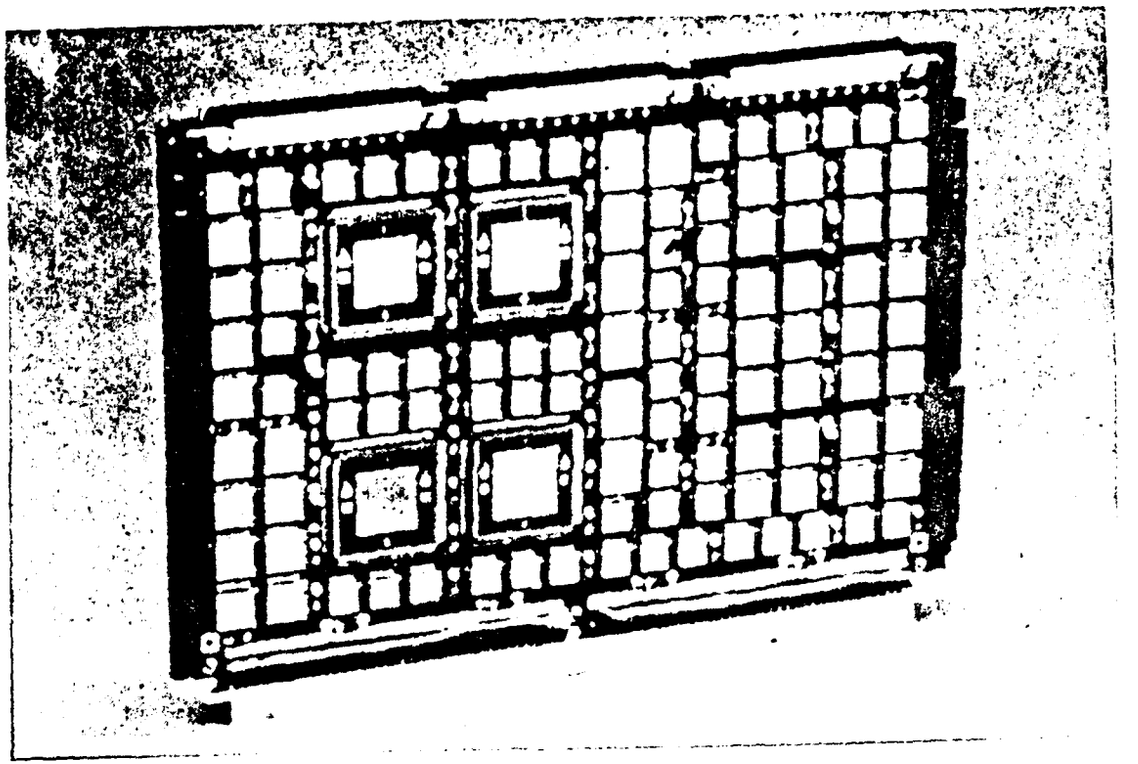

Figure 1. A Typical Surface Mount Assembly

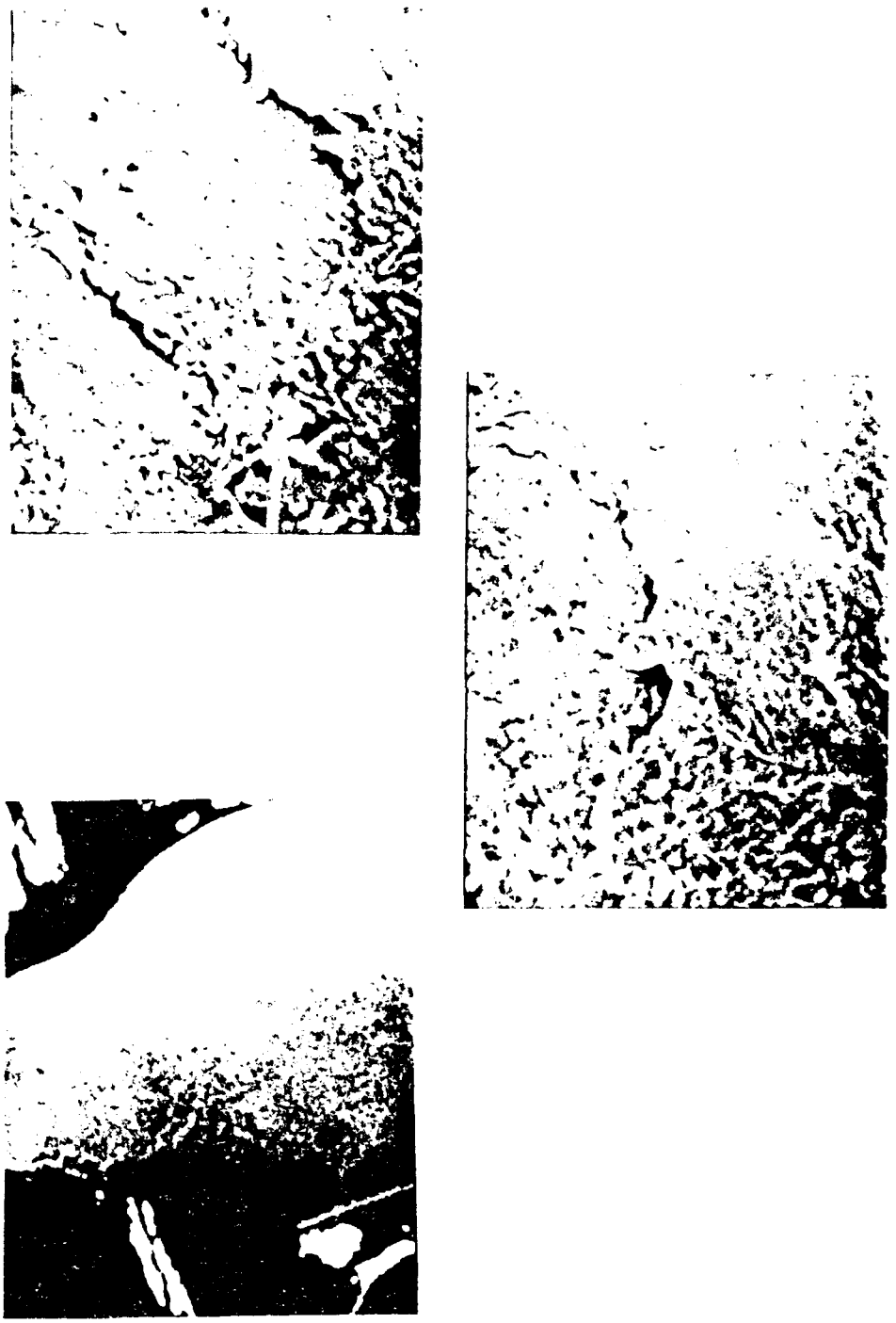

Figure 2A. Three Stages of Solder Joint Degradation
1) LCCC Solder Joint Stress Mark,

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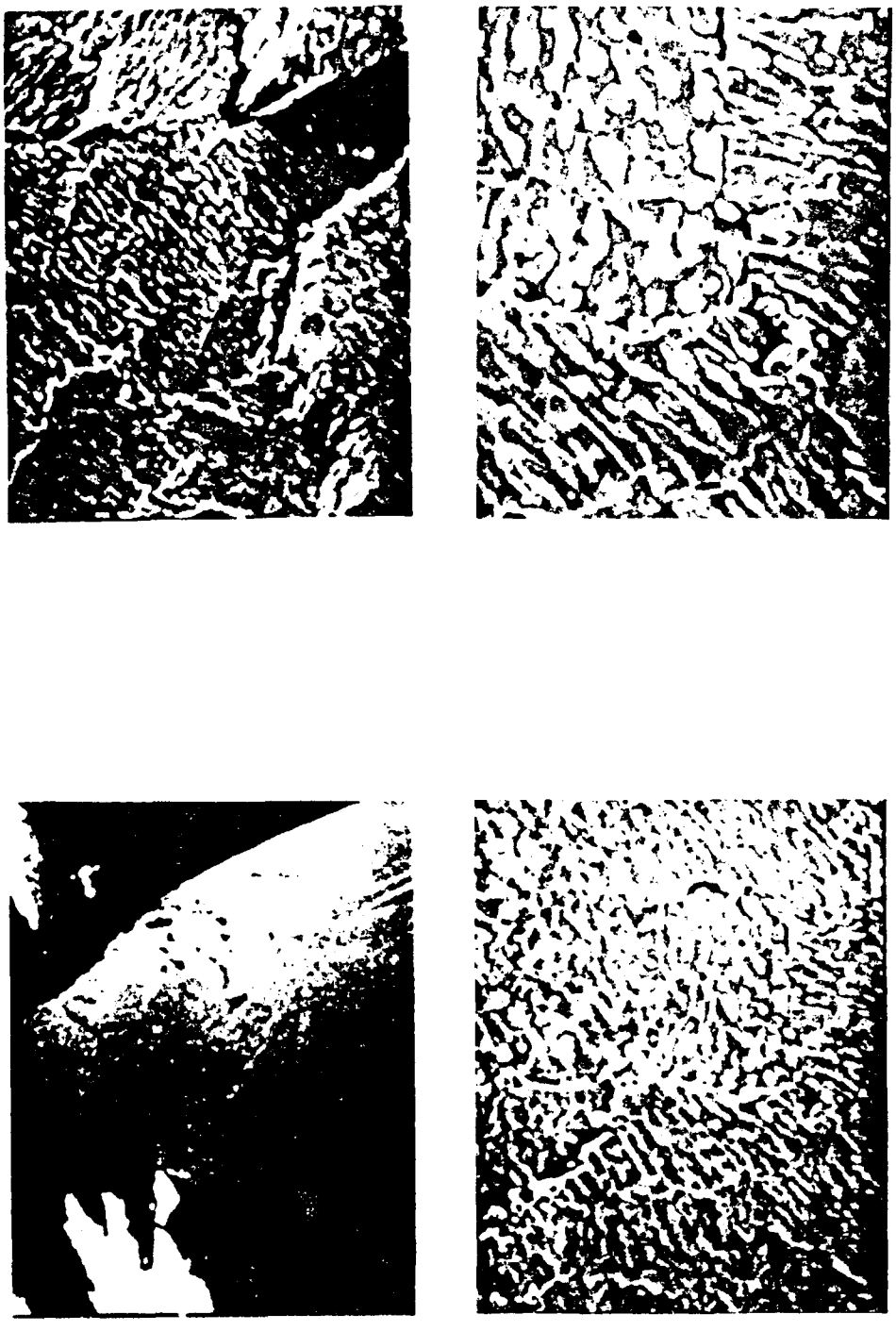

Figure 2B. Three Stages of Solder Joint Degradation
2) LCCC Solder Joint Stress Crack

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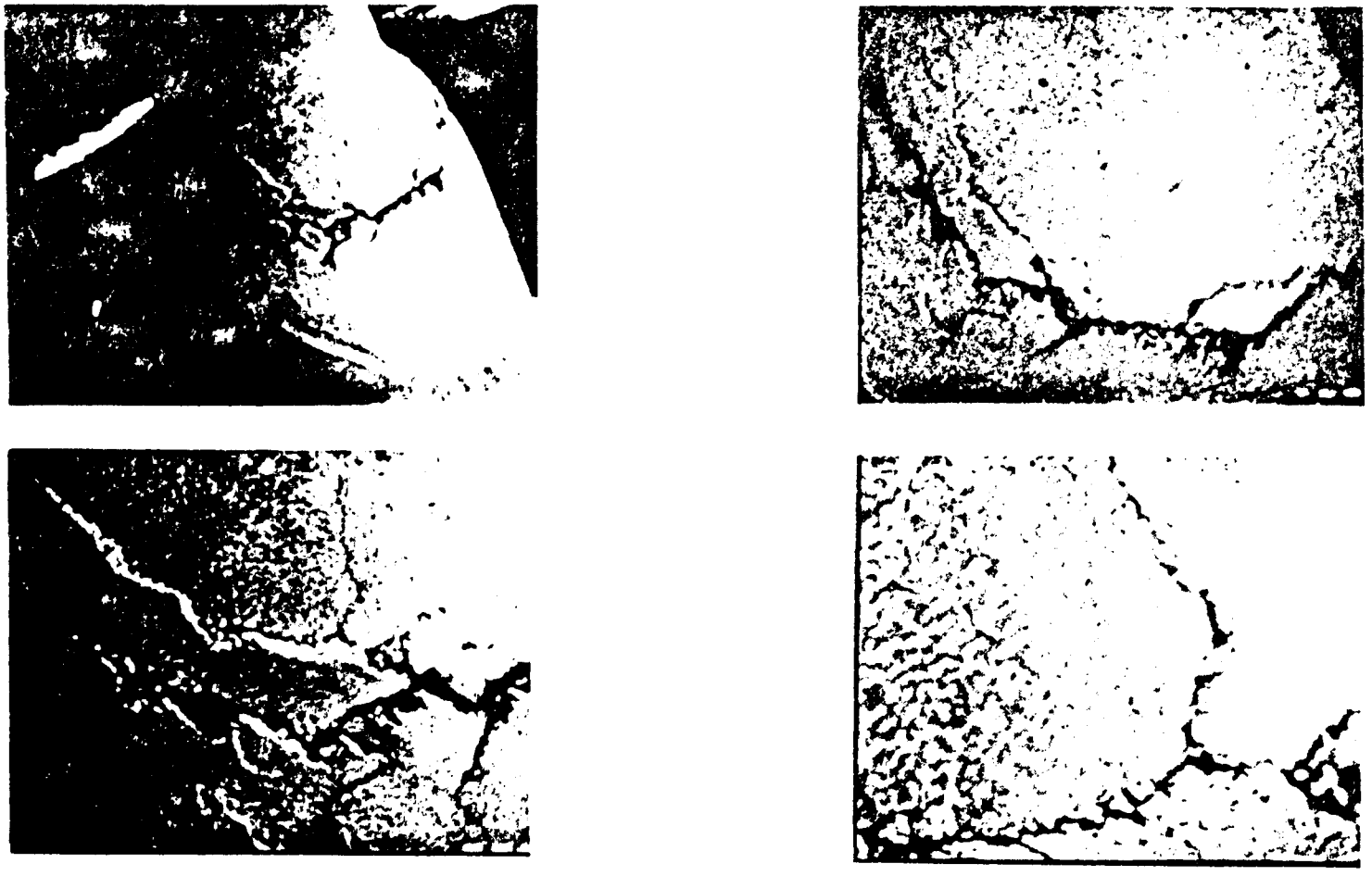

Figure 2C. Three Stages of Solder Joint Degradation
3) LCCC Solder Joint Crack

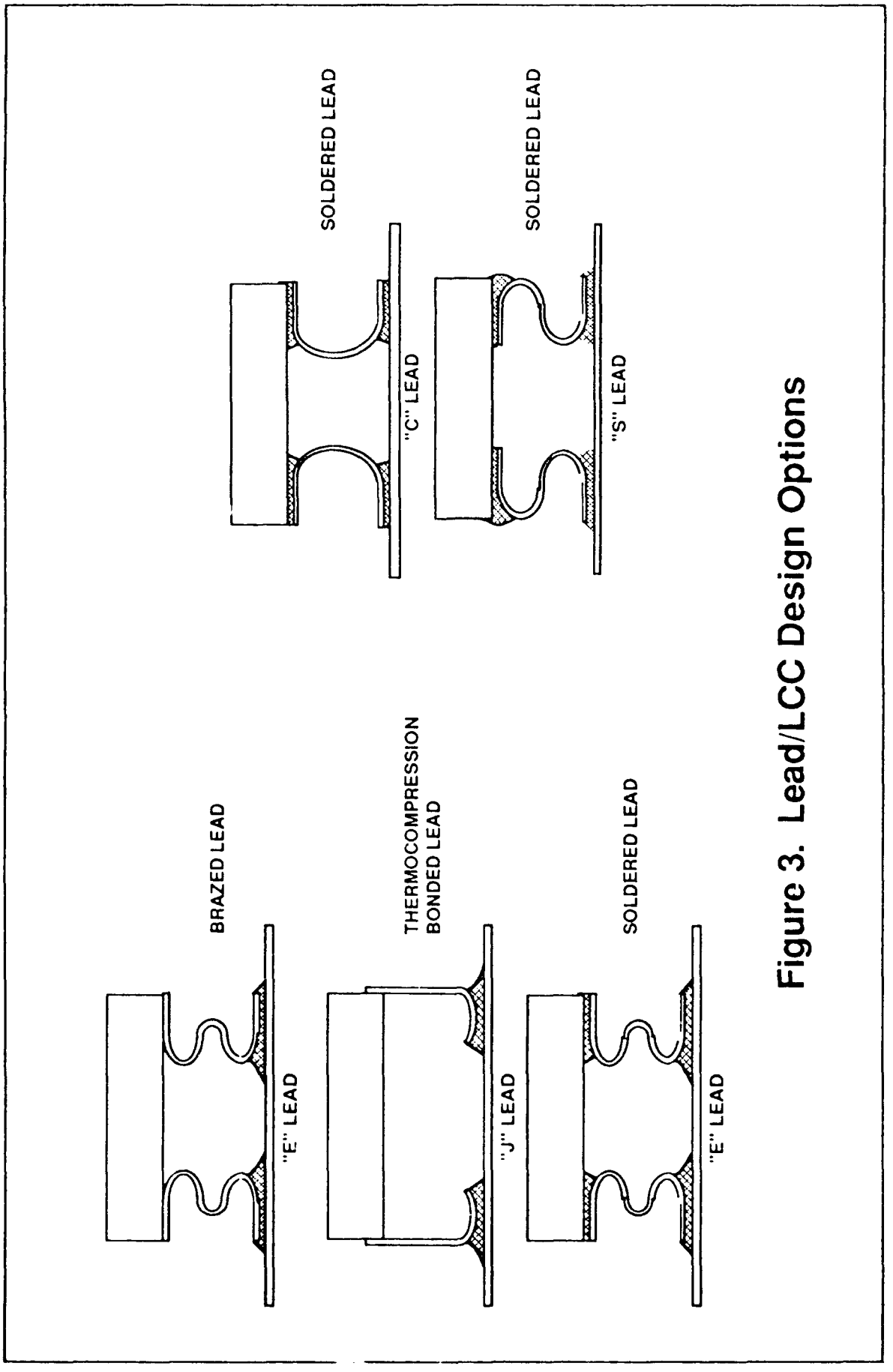

Figure 3. Lead/LCC Design Options

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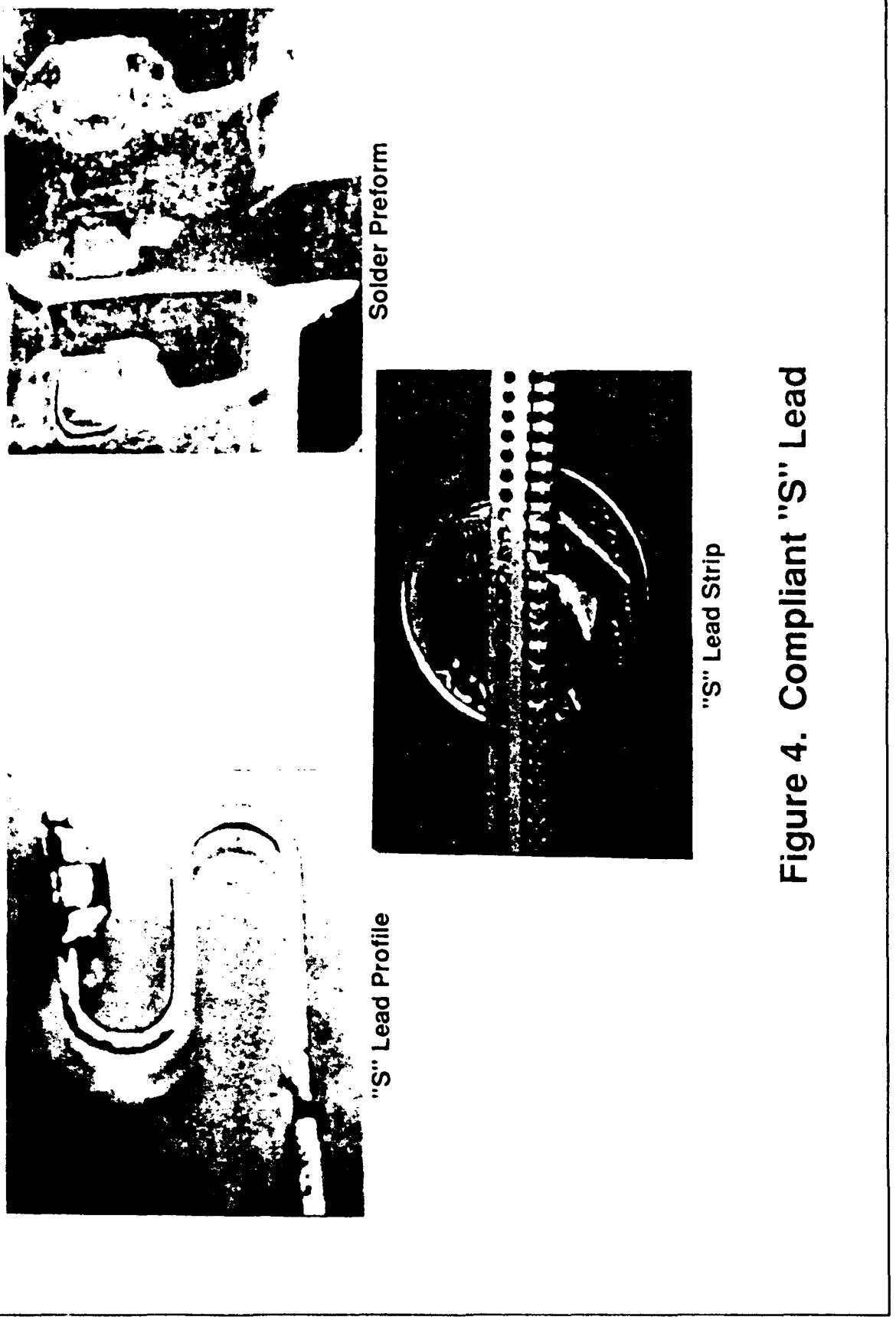

Figure 4. Compliant "S" Lead

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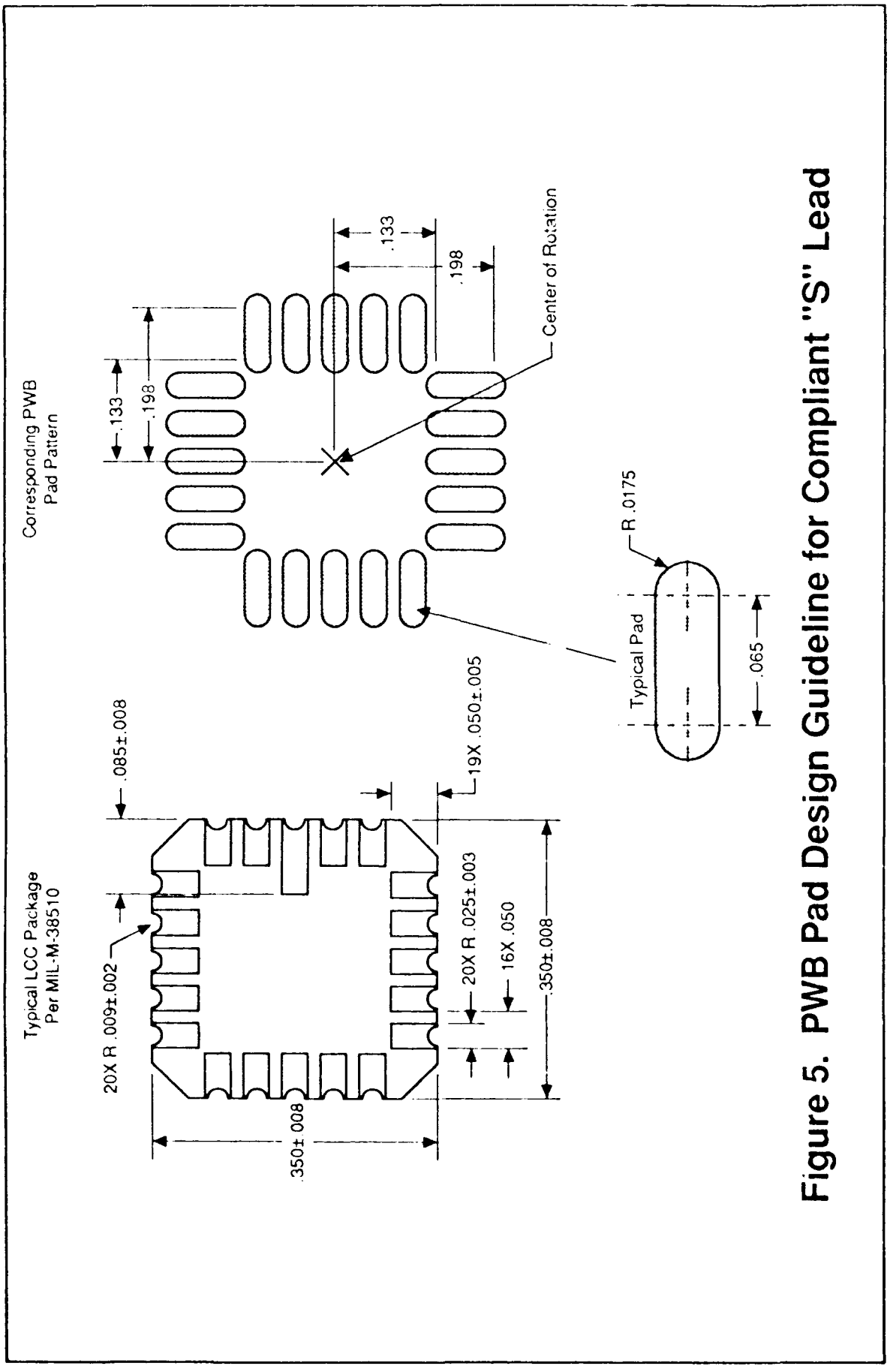

Figure 5. PWB Pad Design Guideline for Compliant "S" Lead

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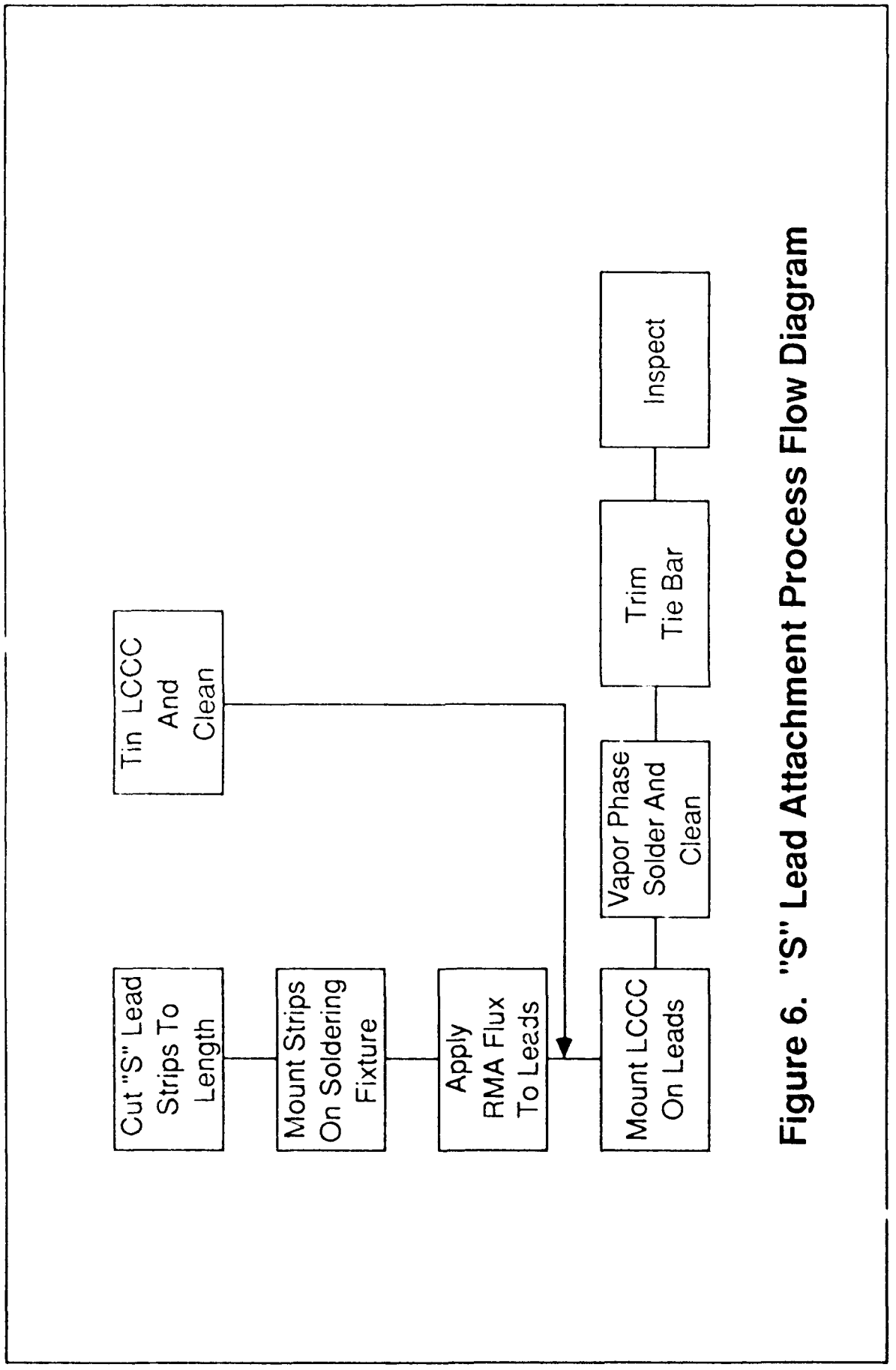

Figure 6. "S" Lead Attachment Process Flow Diagram

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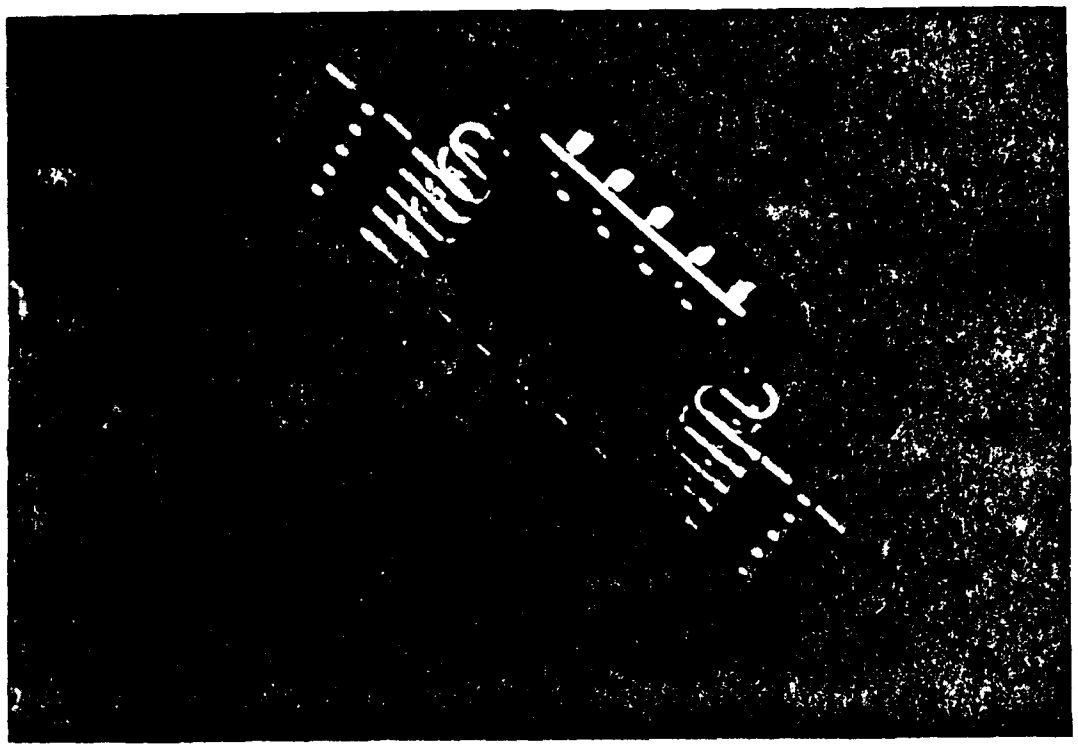

Figure 7. A 20 Pin LCCC with "S" Leads Attached

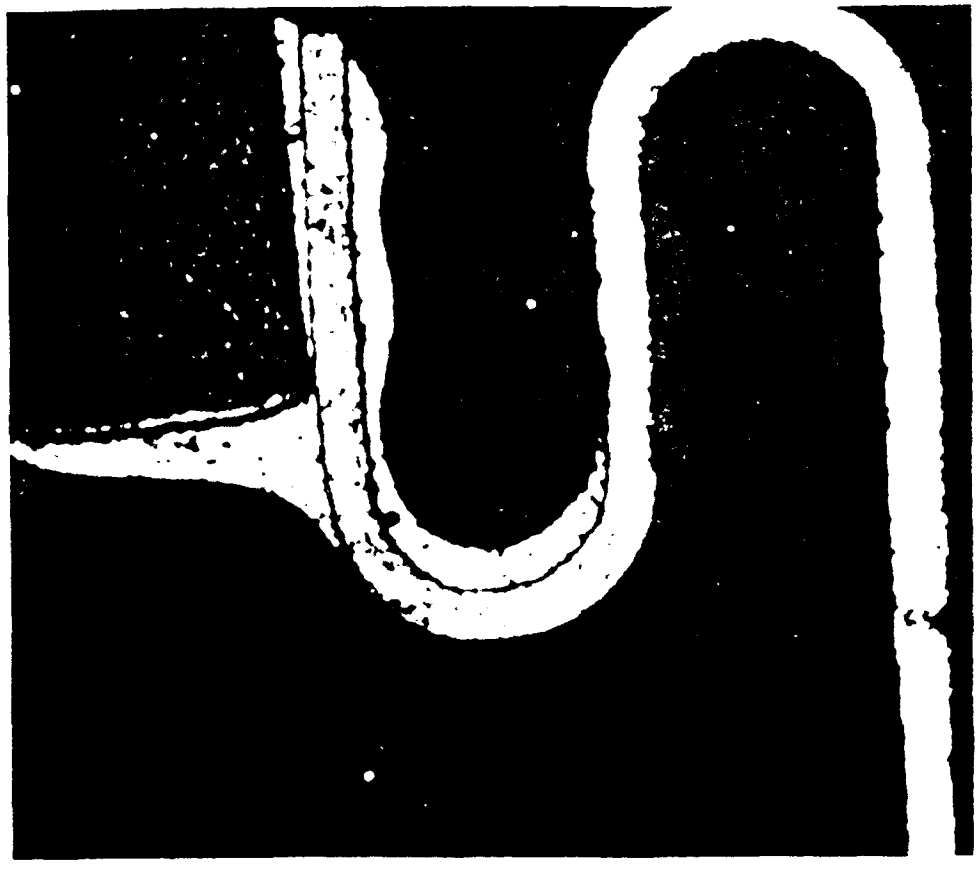

Figure 8. Cross Section – LCCC with "S" Lead

GSRCR-1200(2)

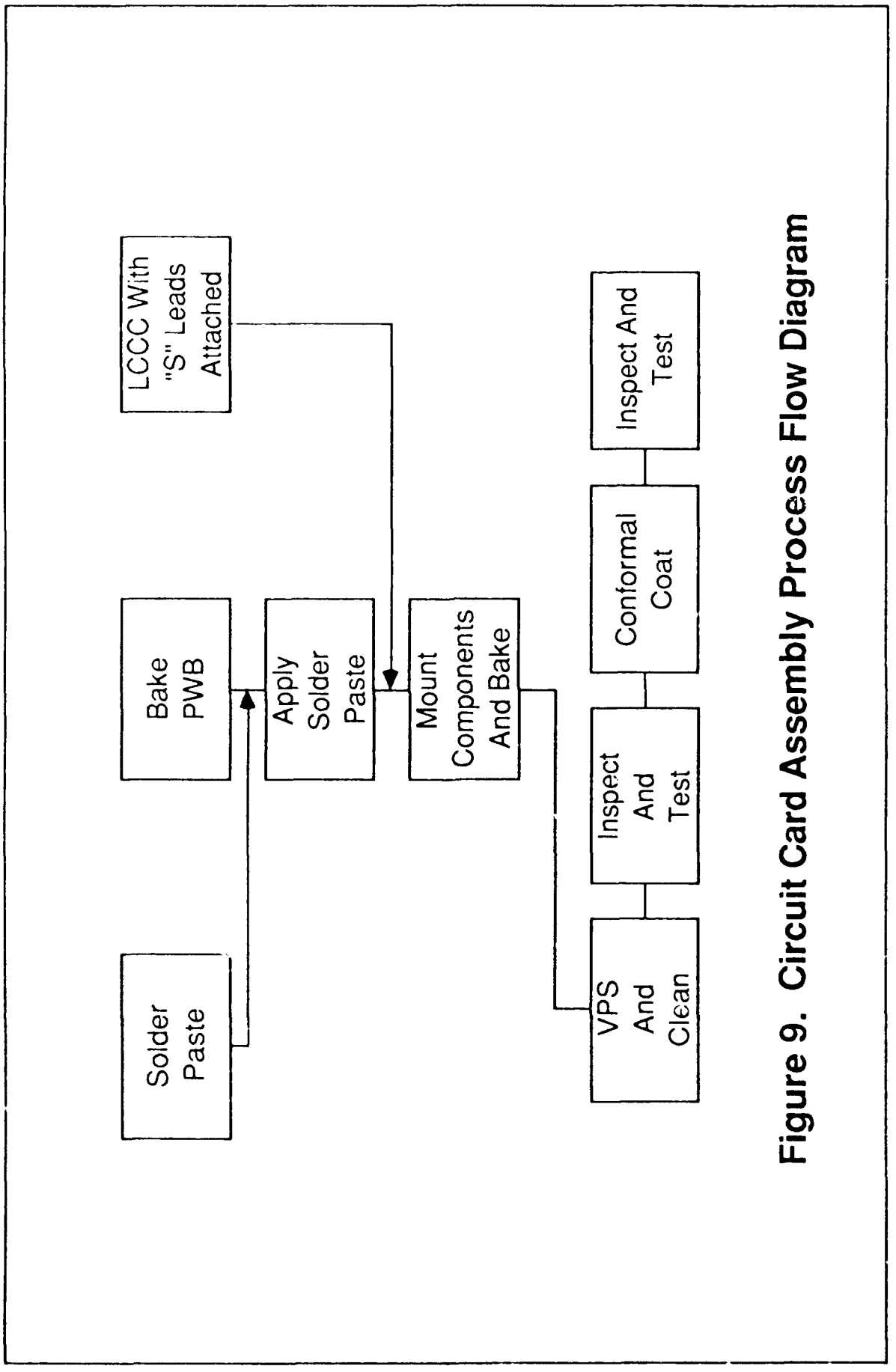

Figure 9. Circuit Card Assembly Process Flow Diagram

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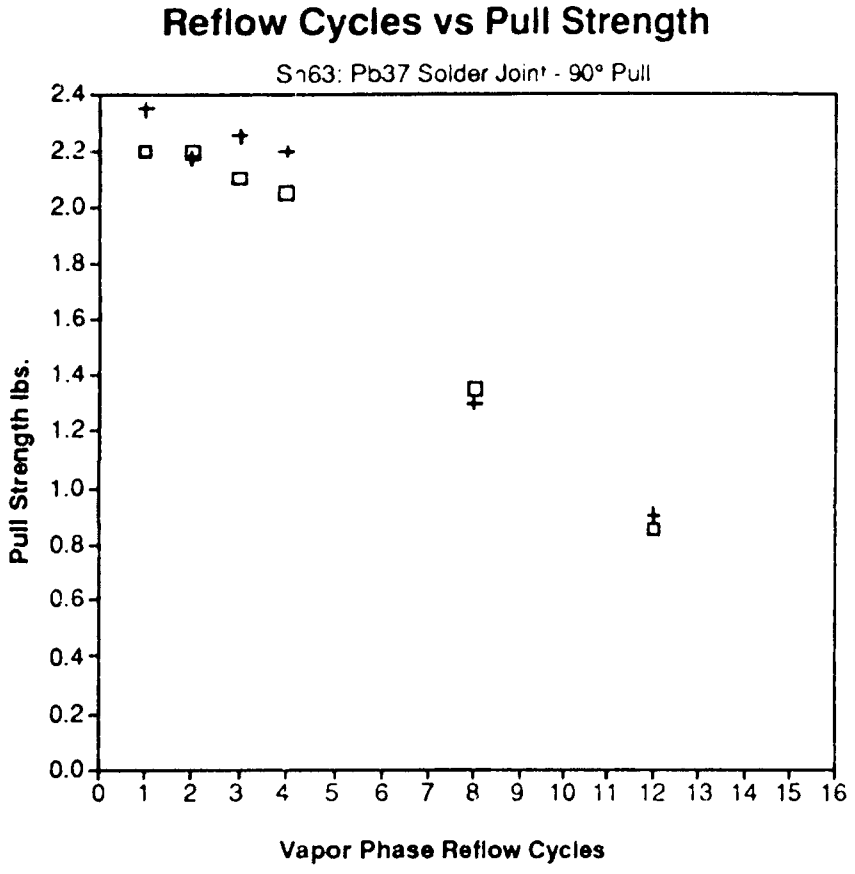

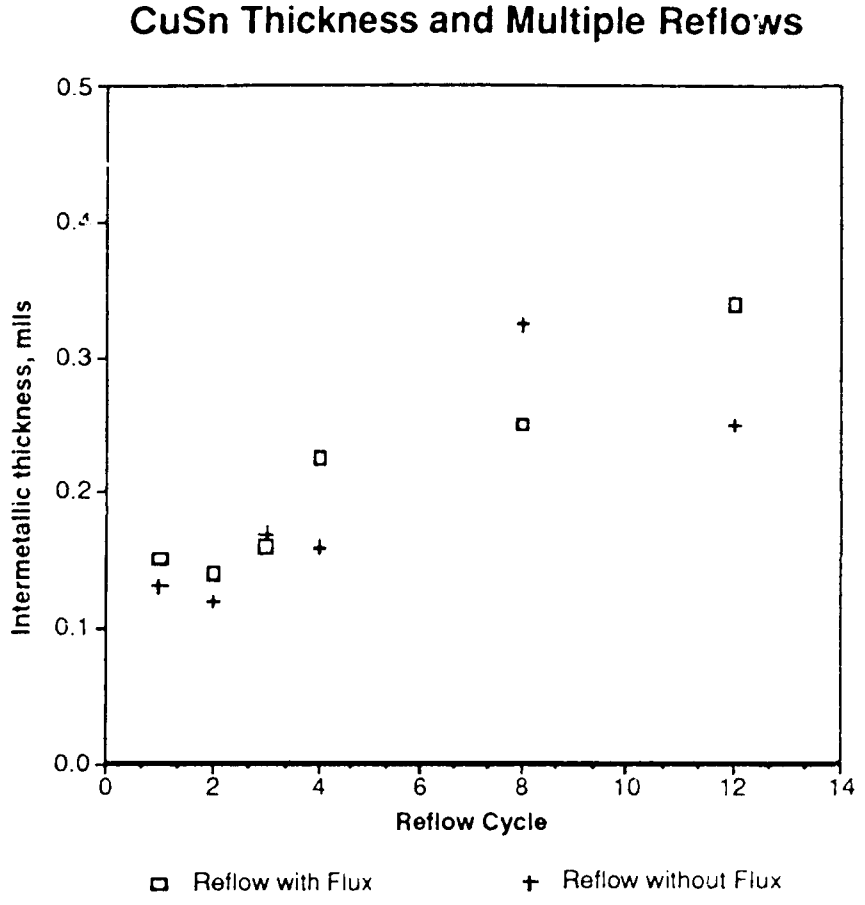

Figure 10. Effect of Multiple Reflow

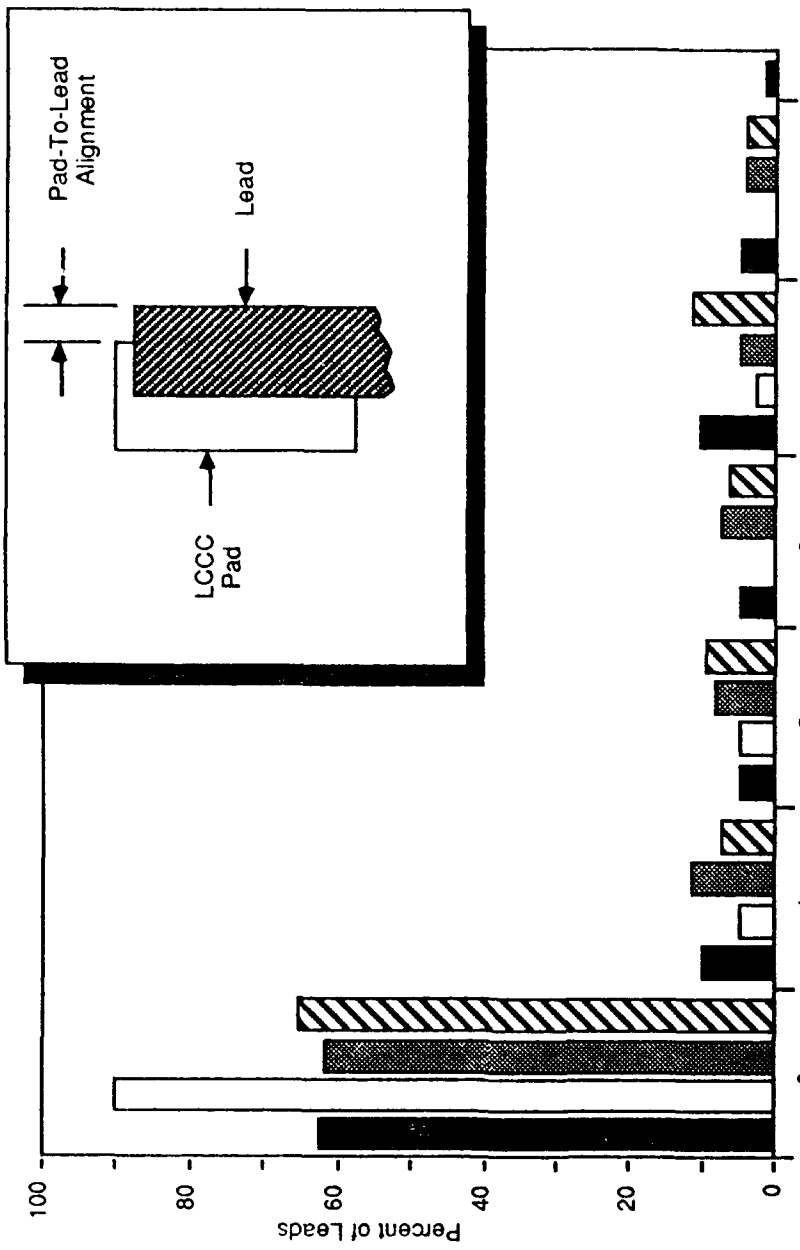

Figure 11. LCCC Pad-to-Lead Alignment After Both Lead Attach and Circuit Card Assembly Reflow

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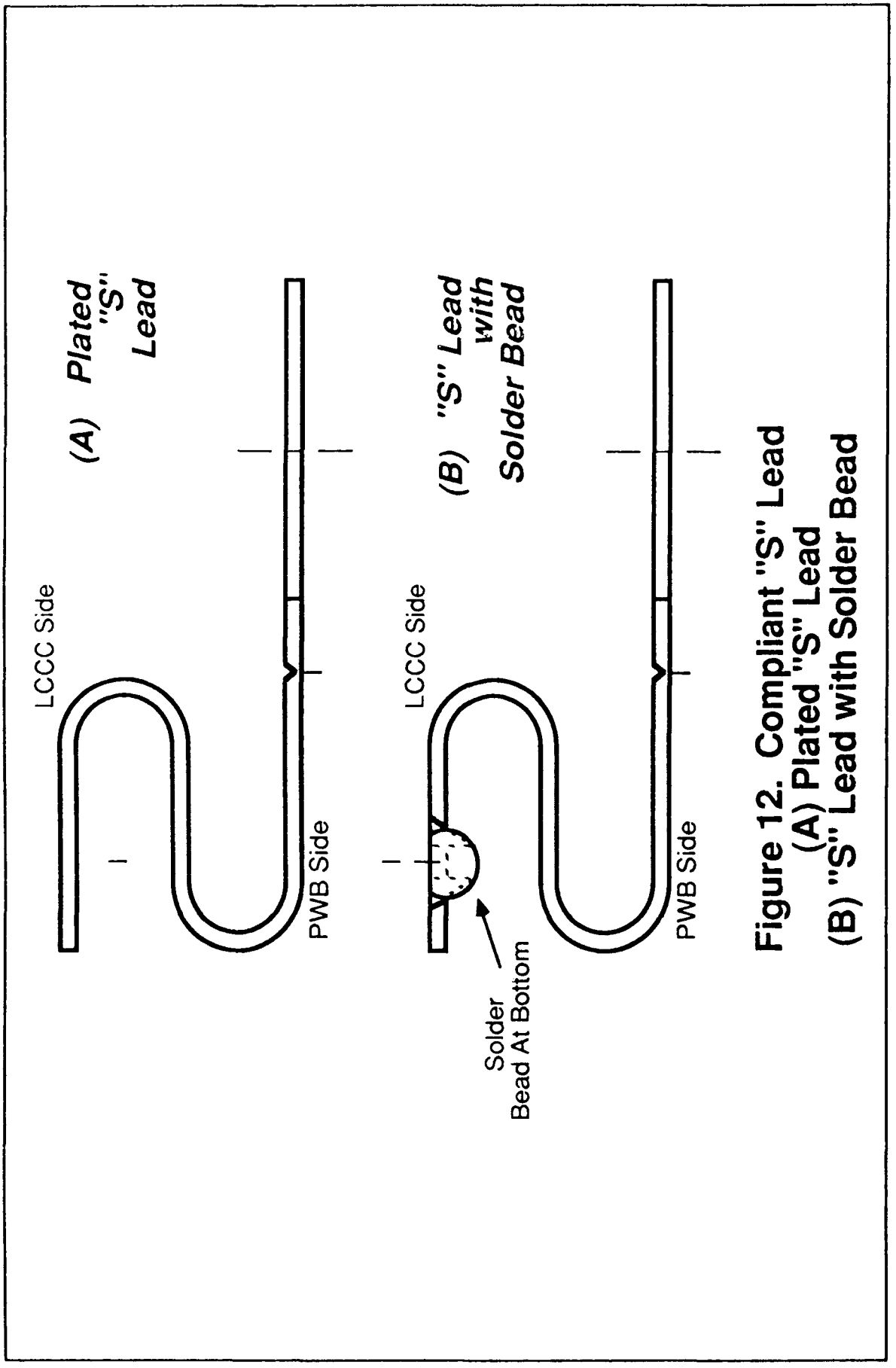

Figure 12. Compliant "S" Lead
(A) Plated "S" Lead
(B) "S" Lead with Solder Bead

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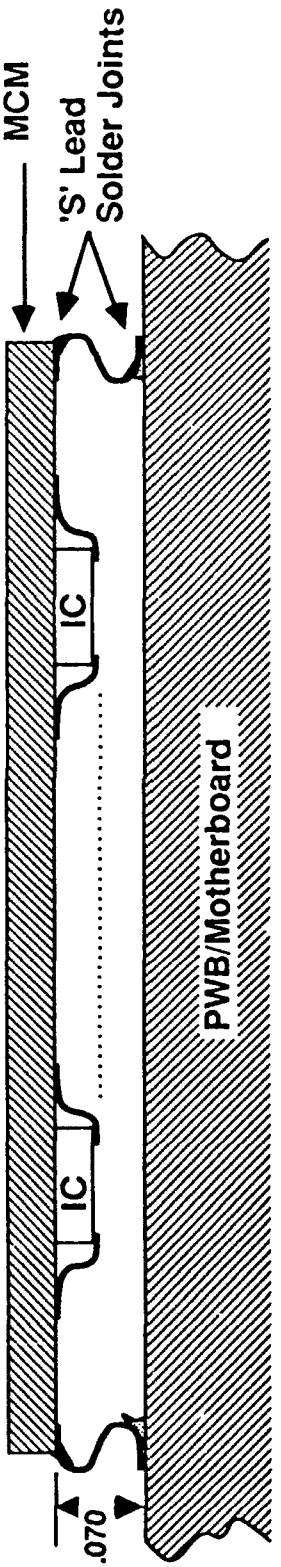

Figure 13. MCM to Motherboard Attachment Using "S" Leads on Four Sides

GSRCR-1200(15)

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ELECTROSTATIC DISCHARGE (ESD) - A HIDDEN THREAT NOW AND LATER

by

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ABSTRACT

This paper is divided into two parts. The first part addresses what ESD is and how it affects ESD-sensitive devices (ESDS devices). The second part deals with implementing an ESD control program within a manufacturing environment.

Both parts are written for compliance to DOD-STD-1686 **Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices).**

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INTRODUCTION

Static Electricity is defined as **Electricity At Rest.** In this state, static electricity poses no threat to harm electronic devices. However, the discharge of that electricity can cause serious damage, even catastrophic failure in extreme cases.

There are two ways by which failure can occur: The first is defined as Conducted Upset, and the second as Radiated Upset. Both of these categories will be discussed in detail later in the paper.

ELECTROSTATIC DISCHARGE

EXAMPLES IN EVERYDAY LIFE

One of the most common examples of ESD is when a person walks across a carpet, touches a doorknob, and gets "zapped". This incident generates a minimum of about 3000 volts, which is the threshold in humans for feeling the discharge of electricity. If more than 5000 volts were generated, a flash of light would be visible if the light were dim enough in the room.

Sliding across a car seat, touching the door handle, and getting "zapped" is another example of ESD in everyday life.

In each of these cases, the ESD is felt, or seen because a charge is generated by rubbing surfaces together, either shoe against carpet or body against seat. Then the charge is discharge via a conductor, the knob in each of the above cases, in connection with the body's "sweat" layer.

MISSILE ACCIDENT - A WORST CASE SCENARIO

In the late 1960's, a missile misfired, killing three people and caused millions of dollars of damage. This was caused by an ESD. A protective cover was pulled off the missile, creating a tremendous static charge. This caused the missile to misfire, wreaking havoc at the site.

MANIFESTATIONS OF ESD SUSCEPTIBILITY

CONDUCTED UPSET

Effects triggered by the direct passage of some portion of the discharge current through the equipment's active or passive components is defined as conducted upset.

RADIATED UPSET

The mode of action is indirect. The equipment is affected by the intense ESD impulse. An example is a failure caused when a spark is drawn to a nearby piece of equipment.

Sometimes there is an apparent overlap between conducted and radiated upset. Consider the situation where a spark is drawn directly to the case of a device in question. ESD current may be diverted to ground so that it does not actually pass through the equipment circuitry. But passage in such close proximity creates very intense transient fields which may cause equipment failure.

PREVENTING CONDUCTED UPSET

Conducted upset occurs when some or all of the ESD passes through the device's electrical circuitry. The currents are extremely intense, reaching peaks as high as 30 amperes in a fraction of a nanosecond. The two approaches available are (1) keep the arc from forming, or (2) if it does, divert it to ground.

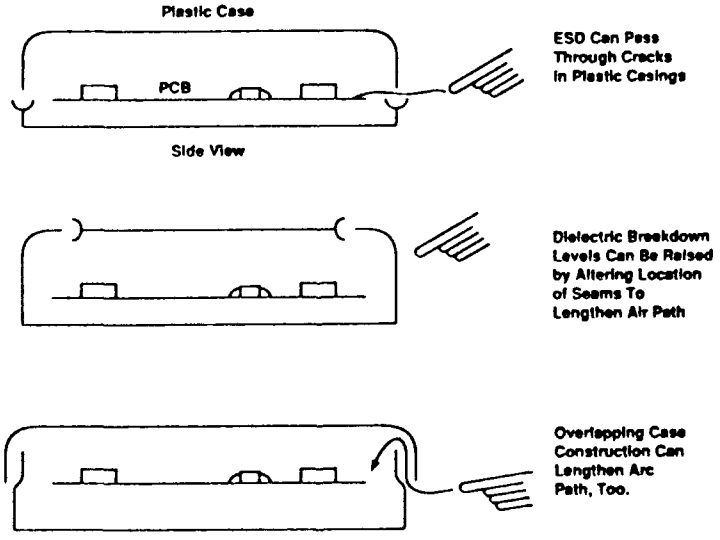

Figure 1 above shows that ESD can pass through seams and openings in an insulating case. The best defense is to prevent the arc from forming by lengthening the minimum distance to the internal circuitry.

CONTROLLING RADIATED UPSET

Radiated upset occurs when the fields generated by the ESD event are picked up by components inside the equipment and misinterpreted as signals. The electric and magnetic fields accompanying the arc may be viewed as having three components: First are near field magnetic components. These fall off as the cube of the distance from the arc. Depending upon the distance from the impulse, magnetic fields induce voltages which can be well in excess of logic thresholds.

Second are near field electric fields: At distances closer to the arc than ($\lambda/2$), the electric field falls off with the square of the distance. Field strengths from ESD events reaching from several hundred to several thousand volts per meter are not uncommon. Circuit leads and attached I/O wires act as antennae. Electric field pickup is especially severe for existing cables.

Third are far field: For distances greater than ($\lambda/2$), both electric and magnetic fields fall off inversely with distance and are coupled together. This is the region of traditional radio propagation.

Controlling radiated upset involves reducing the amount of unwanted signal introduced by a combination of shielding and filtering.

FACTORS AFFECTING ESD

HUMIDITY

This parameter can have a pronounced effect on the discharge of static electricity as shown in Table II below.

TABLE II. Typical electrostatic voltages

Means of Static Generation	Electrostatic Voltages	
	10 to 20 Percent Relative Humidity	65 to 90 Percent Relative Humidity
Walking across carpet	35,000	1,500
Walking over vinyl floor	12,000	250
Worker at bench	6,000	100
Vinyl envelopes for work instructions	7,000	600
Common poly bag picked up from bench	20,000	1,200
Work chair padded with polyurethane foam	18,000	1,500

TRIBOELECTRIC EFFECT

This effect can be generated by rubbing one substance against another, or by pulling two substances apart. A good example of the latter is opening a plastic bag. **Triboelectric** is derived from the Greek, **Tribo** - to rub.

The following Table III is a listing of substances, starting with the most positively charged to the most negative.

TABLE III. Triboelectric Series

Positive (+)	Human Hands
	Glass
	Mica
	Human Hair
	Nylon
	Wool
	Aluminum
	Paper
	Cotton
	Steel
Neutral	Wood
	Hard Rubber
	Nickel, Copper
	Gold, Platinum
	Acetate Rayon
	Polyester
	Orlon
Negative (-)	Polyurethane

GROUNDING OF STATIC ELECTRICAL CHARGE

It is imperative that anyone handling ESDS parts be grounded, preferably with a wrist strap, which is the single most effective defense against ESD.

DESIGN OF ESDS DEVICES

In the design of ESDS devices, it is imperative that ESD-protective circuits be incorporated. Even then, the most sensitive parts (Class 1) can still suffer ESD damage if the electrostatic charge is strong enough.

It is beyond the scope of this paper to elaborate upon the design of microelectronics in detail. Perhaps a paper can be presented which will go into great detail about how these protective circuits are incorporated into parts.

Table IV shows ESDS parts by part type.

CLASS 1: SENSITIVITY RANGE 0 TO $\leq$1000 VOLTS

- Metal Oxide Semiconductor (MOS) devices including C, D, N, P, V and other MOS technology without protective circuitry, or protective circuitry having Class 1 sensitivity.
- Surface Acoustic Wave (SAW) devices
- Operational Amplifiers (OP AMP) with unprotected MOS capacitors
- Junction Field Effect Transistors (JFETs) (Ref.: Similarity to MIL-STD-701: Junction field effect, transistors and junction field effect transistors, dual unitized)
- Silicon Controlled Rectifiers (SCRs) with Io<0.175 amperes at 100° Celsius (°C) ambient temperature (Ref.: Similiarity to MIL-STD-701: Thyristors (silicon controlled rectifiers))
- Precision Voltage Regulator Microcircuits: Line or Load Voltage Regulation <0.5 percent.
- Microwave and Ultra-High Frequency Semiconductors and Microcircuits: Frequency >1 gigahertz
- Thin Film Resistors (Type RN) with tolerance of $\leq$0.1 percent; power >0.05 watt
- Thin Film Resistors (Type RN) with tolerance of >0.1 percent; power $\leq$0.05 watt
- Large scale Integrated (LSI) Microcircuits including microprocessors and memories without protective circuitry, or protective circuitry having Class 1 sensitivity (Note: LSI devices usually have two to three layers of circuitry with metallization crossovers and small geometry active elements)
- Hybrids utilizing Class 1 parts

CLASS 2: SENSITIVITY RANGE >1000 TO $\leq$4000 VOLTS

- MOS devices or devices containing MOS constituents including C, D, N, P, V, or other MOS technology with protective circuitry having Class 2 sensitivity
- Schottky diodes (Ref.: Similarity to MIL-STD-701: Silicon switching diodes (listed in order of increasing trr))
- Precision REsistor Networks (Type RZ)
- High Speed Emitter Coupled Logic (ECL) Microcircuits with propagation delay $\leq$1 nanosecond
- Transistor-Transistor Logic (TTL) Microcircuits (Schottky, low power, high speed, and standard)
- Operational Amplifiers (OP AMP) with MOS capacitors with protective circuitry having Class 2 sensitivity
- LSI with input protection having Class 2 sensitivity
- Hybrids utilizing Class 2 parts

CLASS 3: SENSITIVITY RANGE >4000 TO ≤15,000 VOLTS

- Lower Power Chopper Resistors (Ref.: Similarity to MIL-STD-701: Silicon Low Power Chopper Transistors)
- Resistor Chips
- Small Signal Diodes with power ≤1 watt excluding Zeners (Ref.: Similarity to MIL-STD-701: Silicon Switching Diodes (listed in order of increasing trr))
- General Purpose Silicon Rectifier Diodes and Fast Recovery Diodes (Ref.: Similarity to MIL-STD-701: Silicon Axial Lead Power Rectifiers, Silicon Power Diodes (listed in order of maximum DC output current), Fast Recovery Diodes (listed in order of trr))
- Low Power Silicon Transistors with power ≤5 watts at 25°C (Ref.: Similarity to MIL-STD-701: Silicon Switching Diodes (listed in order of increasing trr), Thyristors (bi-directional triodes), Silicon PNP Low-Power Transistors (Pc ≤5 watts @ T_A = 25°C), Silicon RF Transistors)
- All other Microcircuits not included in Class 1 or Class 2
- Piezoelectric Crystals
- Hybrids utilizing Class 3 parts

DAMAGE TO COMPONENTS

The title of the paper "ESD - A Hidden Threat - Now and Later" will now be explained.

Many times an ESD event may only damage a device on a printed wiring assembly or a circuit trace so slightly that it will remain undetected through in-process testing, final testing, and even operation in the field. Sometimes this can be several years. The damage may even remain undetected indefinitely.

Figure 1 shows damage to circuit traces

ESTABLISHING AND IMPLEMENTING AN ESD CONTROL PROGRAM

GENERAL

Before we go any further, let it be stated that what I will attempt to accomplish is describe in some detail how to establish an ESD control program within a manufacturing environment to comply with DOD-STD-1686. There will be, due to limitation of presentation time, and length of this paper, requirements of the above standard that must go without discussion. The important points, however, will be covered.

There are basically three elements of an ESD-controlled environment: (1) The facility, (2) Personnel, and (3) Handling of ESDS devices during inspection, assembly, and test.

A word of caution is appropriate at this time. DOD-STD-1686 delineates quite well what is required for an ESD control program. DOD-HDBK-263 does a credible job of explaining how -1686 is to be implemented. Keep in mind that -263 only gives guidelines and is not **the** way to implement -1686. The person(s) involved in implementing the program should not fall into the trap of doing **exactly** what -263 says.

Let me illustrate with an example: Air ionizers are a very useful item in neutralizing the air at a work station. These are particularly useful for low humidity conditions (<40% R.H.). However, they are expensive and can cool the air during soldering. If humidity is already controlled, when it drops below 40% R.H., this would probably be an unnecessary expense.

TEMPERATURE AND HUMIDITY CONTROL

Temperature should be maintained between 70-85°F (21-29°C). Humidity should be above 40% R.H. and less than 70% R.H.

PROTECTED AREAS

Electrostatic voltages in areas where Class 1 and Class 2 devices are handled without ESD protective covering shall be limited to the lowest voltage sensitivity level of these devices as a minimum. For example, electrostatic voltages on **operators** and **work areas** shall be kept below 4,000 volts when an equipment cabinet with electrical terminals sensitive to 4,000 volts is being handled without ESD protective covering. Protected areas shall extend, as a minimum, 1 meter from the periphery of a Class 1 or Class 2 device work area. A typical ESD grounded work station is shown in below diagram, Figure 2.

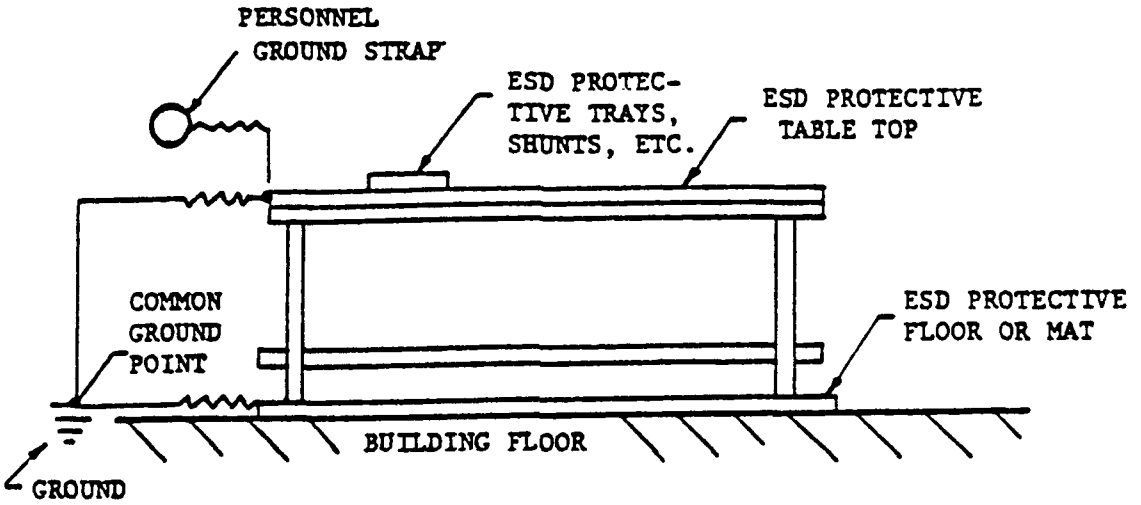

FIGURE 2. Typical ESD grounded work bench

CONDUCTIVE FLOORS

This feature is very effective in the prevention of ESD **only** if foot straps (heel or toe) are utilized. They should be placed on each foot, and should be tested daily with a continuity tester. In addition, chairs with conductive casters are helpful in conjunction with conductive floors.

Conductive floors are basically of three types. The first is a vinyl floor tile impregnated with a conductive layer such as graphite. The second is a floor covered with a conductive mastic. Third is a standard vinyl floor with a conductive wax. The first alternative is the best because of its being permanent. (No wax must be used on this type of floor.)

THE WRIST STRAP

The wrist strap shown depicted in Figure 2 is most commonly comprised of a metallic wrist band (a flexible watch band), a cord with a snap fastener at the wrist band. Just behind the snap is a 1 megohm (1,000,000 ohm) resistor.

The resistor protects the wearer from high voltages which could pass through his or her body on the way to ground. The wrist strap is in turn attached to a conductive bench mat which is connected to earth ground. The strap must be tested daily on a wrist strap continuity tester. Upon testing, a green light means strap is acceptable, a red light means failure. Some testers also have a yellow light. This means "high resist" and is considered a failure.

Should the strap assembly fail a continuity test, **do not** change straps, but change the cord. Almost always the cord is at fault, **not** the wrist strap itself.

SOLDERING IRONS

Where used, soldering irons should be grounded so that resistance from the tip of the hot iron to ground is less than 20 ohms so that the voltage buildup will be less than 15 volts.

PERSONNEL

Training - Persons handling ESDS devices shall be trained.

Persons handling ESDS devices should wear conductive smocks. Finger cots should be worn if contamination from human contact is a problem. If finger cots are worn, only **conductive** ones are allowed.

When transporting ESDS devices, always put them in a **conductive** tote box with the lid **on**. This acts as a Faraday cage by neutralizing the electrical charge. In other words, the charge is conducted away. Boxes must have an ESD warning sticker.

OTHER

Protected areas must be clearly marked to indicate ESDS parts may be present.

TRAINING OUTLINE (TYPICAL)

A comprehensive ESD training course could include the following:

A. ESD control program (Reference DOD-STD-1686)
   1. Organization and responsibility
   2. Program requirements

B. Principles of static electricity
   1. Definition of static electricity
   2. Causes
   3. Prime electrostatic generators
   4. Triboelectric generation, electrostatic fields and ESD high voltage spark discharge induced EMP
   5. Control methods
      a. Grounding
      b. Protective handling
      c. ESD protective materials
      d. Topical antistats
      e. ESD protective equipment
      f. High humidity
      g. Ionized air

C. Electrical and electronic ESDS items
   1. Definition of ESDS items
   2. How ESDS items are damaged or destroyed
   3. Listing of ESDS part types and parts
   4. ESDS part voltage sensitivity levels
   5. ESD classification techniques

D. ESD protective materials and equipment
   1. ESD protective materials
      a. Types such as conductive, static dissipative, and anti-static
      b. Application considerations
   2. Formed shapes of ESD protective materials
      a. Work bench coverings or pads
      b. Tote boxes, trays, vials, bags, carriers, etc.
      c. Floors, floor mats
   3. Protective personnel apparel
      a. Smocks, gauntlets, gloves, finger cots
      b. Topical anti-static treatment of garments
      c. Conductive shoes, shoe covers, heel grounders
      d. Personnel ground straps such as wrist, ankle, or leg
   4. Shorting bars, clips, conductive foams
   5. Protective equipment
      a. Grounded work bench surfaces
      b. Grounded test equipment, power tools
      c. Grounded solder iron tips solder pots, flow soldering equipment
      d. Grounded chairs and stools
      e. Metallized solder suckers
      f. Ionizers
      g. Static alarm systems, detectors and meters

E. Protected areas and grounded work benches
   1. Design and construction
   2. Prohibitions such as common plastics, synthetics, and other static generators, personnel movements to avoid, and cleaning solutions to avoid
   3. Grounding
      a. Techniques
      b. Grounding safety precautions
   4. Monitoring with electrostatic voltmenters, ohmmeters and meggers

F. ESD in design
   1. Considerations in parts selection
   2. Protective circuitry objectives and techniques

G. Failure analysis techniques

H. Handling precautions and procedures

I. Packaging and shipping of ESDS items

ESD CONTROL PHILOSOPHY

1. TRAIN ALL PERSONNEL WHO ARE ASSOCIATED WITH ESDS ITEMS.

2. GROUND ALL PERSONNEL AND EQUIPMENT.

3. PROTECT ALL ESDS ITEMS WHILE IN STORAGE OR IN TRANSIT.

SOME NOTES ABOUT DOD-STD-1686A

PROTECTED AREAS

There is no 1 meter (1 yard) rule with regard to maintaining voltages below the minimum ESD sensitivity greater than that distance if person is unprotected. This document states that voltages must be kept below minimum sensitivity period!

In other words, no one is allowed **anywhere** in the facility if unprotected.

OTHER REQUIREMENTS NOT IN -1686

ESD Program Plan

One must be submitted

Classification of Parts

Class 1 - 0-1,000 volts
Class 2 - 2000-2,999 volts
Class 3 - 4000-15,999 volts

Design Protection

Required on assemblies of 2000 volts minimum
Required on equipment at 4000 volts minimum

The following are also required:

Preparation of internal quality records
Internal quality reporting
Formal reviews and audits
Part selection
Program reviews
Failure analysis
Data requirements

Bibliography

Standards

Military

MIL-STD-129	Marking for Shipment and Storage
DOD-STD-1686	Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices).
MIL-M-38510	Microcircuits, General Specifications for Marking for shipment and storage

Other

Compliance Engineering Application Note
"Designing for Compliance: Immunity to ESD", **Compliance Engineering**, 1991.

W.H. Hensel. "Avoiding Costly Pitfalls in Establishing an ESD Control Program," in EOS/ESD Symposium Proceedings, 1991.

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SHOCK-EXCITED VIBRATIONS OF FLEXIBLE PRINTED CIRCUIT BOARDS

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ABSTRACT

The primary purpose of the analysis is to determine the maximum accelerations experienced by the electronic components and devices surface mounted on a flexible printed circuit board (PCB) whose support contour is subjected to a suddenly applied constant acceleration or to periodic instantaneous impacts. We show that when this contour is immovable (nondeformable) and the deflections are large, it is important to account for the nonlinear effects which are due to the in-plane ("membrane") forces in the PCB. The nonlinearity of PCB vibrations can possibly result in substantially higher accelerations than those predicted by the linear theory. The obtained formulas enable one to evaluate, in addition to the accelerations, also the lateral displacements (amplitudes) and velocities of the surface-mounted devices, as well as the maximum dynamic stresses in the board. These formulas can be helpful when choosing the appropriate PCB type and dimensions, and the most rational lay-out of the components on the board.

INTRODUCTION

Although cyclic differential thermal expansion is usually regarded as the most typical and the most critical type of loading on electronic equipment, mechanical, and especially dynamic, loading often plays a crucial role in the electrical and mechanical performance and reliability of electronic components and devices [Reference 1,2,3]. Dynamic loading can occur during mechanical handling or accidental misuse of the equipment, during shipment (transportation), or, in military use, even during normal operation of the electronic system [Reference 4]. In the analysis below we evaluate the dynamic response of a flexible printed circuit board (PCB) to the following types of shock loads acting on its support contour: 1) suddenly applied constant acceleration, and 2) repetitive instantaneous impacts. A sudden acceleration occurs, for instance, during launching or maneuvering of a spacecraft or a guided missile. Repetitive impacts can be due to typing, or, in military applications, to machine-gun or rapid-shooting-artillery fire.

The study is aimed primarily at the evaluation of the maximum accelerations acting on the electronic components and devices surface-mounted on the board. In addition, we determine the maximum displacements (amplitudes) and the lateral velocities, as well as the dynamic stresses in the board itself. While elevated accelerations affect the mechanical integrity and normal functioning of the electronic components, the stresses in

the board can cause damage to its structure and shorten the fatigue life.

Our investigation is based on an analytical stress model and considers the fact that the PCB contour is typically immovable (nondeformable). This results in reactive in-plane ("membrane") forces which are proportional to the cube of the deflections (see, for instance, [Reference 5,6]), thereby making the problem nonlinear. Limiting our analysis to the principal mode of vibrations, we obtain the exact solutions to the problems in question. This enables one to apply such solutions with confidence not only when the loads and the deflections are small, but in the case of intensive loading and large deflections as well.

We would like to point out that linear approach, which considers bending only and does not account for the in-plane forces, always overestimates the dynamic deflections (amplitudes) and the bending stresses. However, when the deflections are not small, the linear theory may not be conservative. As far as the stresses are concerned, this is simply due to the membrane stresses which are proportional to the deflections squared and are not accounted for by the linear theory. As to the maximum accelerations, this is due to the fact that the nonlinear vibration frequency can be significantly larger than the linear frequency. Therefore the nonlinear accelerations which are approximately proportional to the frequency of vibrations squared, can exceed considerably the linear accelerations, even despite the fact that the nonlinear amplitudes are relatively small.

From the viewpoint of structural analysis, a PCB can be treated as a thin and flexible rectangular plate. Various linear and nonlinear problems of the dynamics of plate structures were analyzed in numerous monographs, manuals, and reference books (see, for instance, [Reference 7,8,9]). Approximate analyses of nonlinear oscillators with stiff cubic characteristics of nonlinearity (so called, "Duffing oscillators" [Reference 10]) are presented, for instance, in the books by Kauderer [Reference 11] and Hayashi [Reference 12]. It is noteworthy, however, that in these books and manuals the emphasis is on continuous harmonic excitations and "weak" nonlinearities. Solutions to static problems of nonlinear bending of plates were presented by Bubnov [Reference 13], Prescott [Reference 14], Levy [Reference 15,16,17] and others, and can be found in the well-known book by Timoshenko and Woinowski-Krieger [Reference 5]. Linear and nonliner vibrations due to periodic impulses were examined, using different approaches and in application to various engineering problems, by Burton [Reference 18], Panovko and Gubanova [Reference 19], Krajcinovic [Reference 20], Suhir [Reference 21,22,23], Veluswami [Reference 24], Paz and O'Charoen [Reference 25], Halbauer [Reference 26], Hsu, Chen, and Lee [Reference 27] and others. Linear modal analyses and dynamic response predictions for PCB's and surface-mounted components, experiencing dynamic loading, have been carried out recently by Lau and Keely [Reference 28], Covetto, Gupta, and Kim [Reference 29], Keltie and Ozisik [Reference 30], Kim and Gupta [Reference 31], Wong, Stevens, and Wang [Reference 32]. Structural analysis of circuit board (card) systems subjected to bending was performed by Engel [Reference 33].

ANALYSIS

1. Equations of Motion

The kinetic energy T and the strain energy V of a PCB subjected to bending and in-plane forces are expressed as follows [Reference 7]:

$$T = \frac{1}{2} m \int_A \left[\frac{\partial w}{\partial t}\right]^2 dA , \tag{1}$$

$$V = \frac{1}{2} D \int_A [(\Delta w)^2 - 2(1 - \nu) L (w,w)] dA +$$

$$+ \frac{1}{2} \frac{h}{E} \int_A [(\Delta \phi)^2 - 2(1 + \nu) L (\phi,\phi)] dA . \tag{2}$$

Here $A = ab$ is the PCB area, a and b are PCB dimensions in the x and y directions, respectively (Fig. 1), m is the board's mass per unit area (with consideration of the masses of the surface mounted components, assuming that these masses can be uniformly "spread" on the PCB surface), $D = Eh^3/12(1-\nu^2)$ is the PCBs flexural rigidity (we assume that the components surface mounted on the broad are sufficiently small in size and affect only the PCB mass, but not its rigidity), h is the board's thickness, E is Young's modulus of the material, ν is Poisson's ratio, $w = w(x,y,t)$ is the deflection function, $\phi = \phi(x,y,t)$ is the stress (Airy) function,

$$\Delta = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}$$

is the Laplace operator, and the operator L is as follows:

$$L = \frac{\partial^2}{\partial x^2} \frac{\partial^2}{\partial y^2} - \left[\frac{\partial^2}{\partial x \partial y}\right]^2 .$$

The first term in (2) is due to bending, and the second term is due to tensile in-plane forces. Note that although the elastic constants of the PCB are somewhat different in the x and y directions, in this study we do not account for such a difference.

Limiting our analysis to the fundamental mode of vibrations, we present the functions w and ϕ in the form:

$$w = w_c(t) - w_1(x,y)z(t), \quad \phi = \phi_1(x,y)z^2(t) , \tag{3}$$

where $w_c(t)$ is the displacement of the support contour, $w_1(x,y)$ is the coordinate function of the fundamental mode, $z(t)$ is the corresponding principal coordinate, and $\phi_1(x,y)$ is the static stress function. For a simply supported board of finite aspect ratio b/a, changing within the range between 1 and 2, the function w_1 can be presented as

$$w_1 = \cos \frac{\pi x}{a} \cos \frac{\pi y}{b} , \tag{4}$$

and the static stress function for a board with an immovable support contour is [Reference 14]:

$$\phi_1 = \frac{E}{32}\left\{\frac{2\pi^2}{1-\nu^2}\left[\left(\frac{\nu}{a^2}+\frac{1}{b^2}\right)x^2+\left(\frac{1}{a^2}+\frac{\nu}{b^2}\right)y^2\right]\right.$$

$$\left. -\frac{a^2}{b^2}\cos\frac{\pi x}{a}-\frac{b^2}{a^2}\cos\frac{\pi y}{b}\right\} \qquad (5)$$

The coordinate function for a clamped board, having an aspect ratio b/a between 1 and 1.5, can be assumed in the following approximate form [Reference 17]

$$w_1 = \cos^2\frac{\pi x}{a}\cos^2\frac{\pi y}{b}\ . \qquad (6)$$

This results in the following expression for the static stress function $\phi_1(x,y)$:

$$\phi_1 = \frac{E}{32}\left\{\frac{3\pi^2}{2(1-\nu^2)}\left[\left(\frac{\nu}{a^2}+\frac{1}{b^2}\right)x^2+\left(\frac{1}{a^2}+\frac{\nu}{b^2}\right)y^2\right.\right.$$

$$-\frac{a^2}{b^2}\cos\frac{\pi x}{a}-\frac{b^2}{a^2}\cos\frac{\pi y}{b}-\left[\frac{a}{4b}\right]^2\cos\frac{4\pi x}{a}$$

$$-\left[\frac{b}{4a}\right]^2\cos\frac{4\pi y}{b}-\frac{2a^2b^2}{(a^2+b^2)^2}\cos\frac{2\pi x}{a}\cos\frac{2\pi y}{b}-$$

$$-\frac{a^2b^2}{(4a^2+b^2)^2}\cos\frac{2\pi x}{a}\cos\frac{4\pi y}{b}$$

$$\left.\left.-\frac{a^2b^2}{(a^2+4b^2)^2}\cos\frac{4\pi x}{a}\cos\frac{2\pi y}{b}\right\}\ . \qquad (7)$$

In the case of an elongated board, the coordinate function w_1 is [Reference 5,6]

$$w_1 = C \cos \beta \frac{x}{a} + \cos \beta \frac{x}{a} , \tag{8}$$

where $C = 0$, $\beta = \pi$ for a simply supported board, and $C = 0.1329$, $\beta = 4.73$ for a clamped board.

Substituting (3) into (1) and (2), we obtain:

$$T = \frac{1}{2} \left[m\dot{w}_c^2 A - 2 M_0 \dot{w}_c \dot{z} + M\dot{z}^2 \right] , \tag{9}$$

$$V = \frac{1}{2} M \left[\lambda_0^2 z^2 + \frac{1}{2} \alpha z^4 \right] , \tag{10}$$

where

$$M_0 = m \int_A w_1 \, dA \tag{11}$$

is the generalized mass associated with the excitation force,

$$M = m \int_A w_1^2 \, dA \tag{12}$$

is the generalized mass associated with the vibration system itself,

$$\lambda_0 = \sqrt{\frac{D}{M} \int_A \left[(\Delta w_1)^2 - (1 - \nu) L (w_1, w_1) \right] dA} \tag{13}$$

is the linear natural frequency of the board, and

$$\alpha = \frac{2h}{EM} \int_A \left[(\Delta \phi_1)^2 - 2(1 + \nu) L (\phi_1, \phi_1) \right] dA \tag{14}$$

is the parameter of nonlinearity of vibrations. Introducing the formulas (9) and (10) in the Lagrange equation (see, for instance, [Reference 34])

$$\frac{d}{dt} \frac{\partial T}{\partial \dot{z}} + \frac{\partial V}{\partial z} = 0 ,$$

we obtain:

$$\ddot{z} + \lambda_0^2 z + \alpha z^3 = \frac{Q(t)}{M} , \tag{15}$$

where

$$Q(t) = M_0 \ddot{w}_c(t) \tag{16}$$

is the excitation force.

If the force $Q(t)$ is due to a constant acceleration $\ddot{w}_c$ applied to the support contour, than this force is constant and is $Q = M_0 \ddot{w}_c$. In this case the equation (15) can be written as follows:

$$\ddot{z} + \lambda_0^2 z + \alpha z^3 = q\,, \tag{17}$$

where $q = c\ddot{w}_c = \text{const}$, and the ratio

$$c = \frac{M_0}{M} = \frac{\int_A w_1\, dA}{\int_A w_1^2\, dA} \tag{18}$$

considers the effect of the coordinate function on the excitation force. If the force $Q(t)$ is due to repetitive instantaneous impacts, causing the change in the contour's velocity by the amount $\dot{w}_c$, then this force can be presented in the form of a series

$$Q(t) = P \sum_{k=0}^{n} \delta(t - kT_s), \quad n = 0, 1, 2, \cdots \tag{19}$$

where

$$P = M_0 \dot{w}_c$$

is the generalized impulse, $\delta(t)$ is Dirac's delta-function (see, for instance, [Reference 35]), and T_s is the time between the impacts. Then the equation (11) can be written as

$$\ddot{z} + \lambda_0^2 z + \alpha z^3 = \frac{P}{M} \sum_{k=0}^{n} \delta(t - kT_s), \quad n = 0, 1, 2, \cdots \tag{20}$$

This equation describes the PCB vibrations after the n-th impact is applied.

2. Coefficients in the Equations of Motion

After introducing (4) and (5) into the formulas (11), (12), (13), and (14), we obtain the following expressions for the generalized masses M_0 and M, linear frequency λ_0, and the parameter α of nonlinearity: for a simply supported PCB:

$$\left.\begin{aligned} M_0 &= \frac{4}{\pi^2}\, mA, \quad M = \frac{1}{4}\, mA, \\ \lambda_0 &= \pi^2 \frac{a^2 + b^2}{a^2 b^2} \sqrt{\frac{D}{m}}, \\ \alpha &= \frac{3\pi^4 D}{4mh^2} \frac{(3 - \nu^2)(a^4 + b^4) + 4\nu a^2 b^2}{a^4 b^4} \end{aligned}\right\} \tag{21}$$

In the case of a square board ($a = b$), the formulas for the frequency λ_0 and the parameter α can be simplified:

$$\lambda_0 = \frac{2\pi^2}{a^2}\sqrt{\frac{D}{m}}, \quad \alpha = \frac{\pi^4}{8}\,\frac{3-\nu}{1-\nu}\,\frac{Eh}{ma^4} \tag{22}$$

Similarly, using the formulas (6) and (7), we obtain the following values of the parameters M_0, M, λ_0, and α for a clamped board:

$$\left.\begin{aligned} M_0 &= \frac{1}{4}\,mA, \quad M = \frac{9}{64}\,mA, \\ \lambda_0 &= \frac{4\pi^2}{3a^2b^2}\sqrt{[3(a^4+b^4)+2a^2b^2]\,\frac{D}{m}}, \\ \alpha &= \frac{\pi^4 Eh}{18ma^4b^4}\left[\frac{9(a^4+b^4+2\nu a^2b^2)}{4(1-\nu^2)}\right. \\ &\quad + \frac{17}{8}(a^4+b^4) + \frac{12a^4b^4}{(a^2+b^2)^2} + \\ &\quad \left. + \frac{5a^4b^4}{(4a^2+b^2)^2} + \frac{5a^4b^4}{(a^2+4b^2)^2}\right] \end{aligned}\right\} \tag{23}$$

For a square board ($a = b$)

$$\lambda_0 = \frac{8\pi^2}{3a^2}\sqrt{\frac{2D}{m}}, \quad \alpha = \frac{\pi^4}{40}\,\frac{27-17\nu}{1-\nu}\,\frac{Eh}{ma^4} \tag{24}$$

In the case of an elongated simply supported board, using the expression (8), with $C = 0$ and $\beta = \pi$, we obtain:

$$\left.\begin{aligned} M_0 &= \frac{2}{\pi}\,ma, \quad M = \frac{1}{2}\,ma, \quad \lambda_0 = \frac{\pi^2}{a^2}\sqrt{\frac{D}{m}} \\ \alpha &= 3\,\frac{\lambda_0^2}{h^2} = 292\,\frac{D}{h^2a^4m} \end{aligned}\right\} \tag{25}$$

In the case of a clamped board, when $C = 0.1329$ and $\beta = 4.73$, we obtain:

$$\left.\begin{aligned} M_0 &= 0.593\ ma,\quad M = 0.509\ ma, \\ \lambda_0 &= \frac{10}{a^2}\sqrt{\frac{5D}{m}}\quad \alpha = 0.282\ \frac{\lambda_0^2}{h^2} = 141\ \frac{D}{h^2 a^4 m} \end{aligned}\right\} \tag{26}$$

3. Constant Suddenly Applied Acceleration

3.1 Maximum Deflection, Velocity, and Acceleration

The maxima of the deflection, velocity, and acceleration can be determined even without solving the equation (17), i.e. without obtaining the PCB responses as functions of time. Indeed, with the constant q value, this equation can be written as

$$\frac{d}{dt}\left(\dot{z}^2 + \lambda_0^2 z^2 + \frac{1}{2}\alpha z^4 - 2qz\right) = 0\ ,$$

or

$$\dot{z}^2 + \lambda_0^2 z^2 + \frac{1}{2}\alpha z^4 - 2qz = C\ .$$

If the initial displacement and the initial velocity of the PCB are zero, the constant of integration C is also zero, and therefore

$$\dot{z} = \sqrt{2qz - \lambda_0^2 z^2 - \frac{1}{2}\alpha z^4}\ . \tag{27}$$

This relationship (phase diagram) is plotted in Fig. 2.

The displacement z reaches its maximum value z_{max} at the end of the first quarter-period of vibrations, when the induced (relative) velocity is zero. This results in the equation:

$$2q - \lambda_0^2 z_{max} - \frac{1}{2}\alpha z_{max}^3 = 0\ . \tag{28}$$

If the force q were applied statically, then, putting in the equation (17) $\ddot{z} = 0$, we obtain the following cubic equation for the relative static displacement z_{st}:

$$q - \lambda_0^2 z_{st} - \alpha z_{st}^3 = 0\ . \tag{29}$$

Since the maximum relative velocity $\dot{z}_{max}$ also takes place when the acceleration $\ddot{z}$ is zero, we conclude, that $\dot{z} = \dot{z}_{max}$, when $z = z_{st}$, so that

$$\dot{z}_{max} = \sqrt{2qz_{st} - \lambda_0^2 z_{st}^2 - \frac{1}{2}\alpha z_{st}^4}\ . \tag{30}$$

The cubic equations (28) and (29) have the following solutions:

$$z_{max} = \eta_z \, z^0_{max} \, , \tag{31}$$

$$z_{st} = \eta_{st} \, z^0_{st} \, , \tag{32}$$

where

$$z^0_{max} = \frac{2q}{\lambda_0^2} \tag{33}$$

is the maximum linear dynamic displacement,

$$z^0_{st} = \frac{q}{\lambda_0^2} = \frac{1}{2} \, z^0_{max} \tag{34}$$

is the maximum linear static displacement (which is twice as small as the dynamic displacement) and the factors

$$\left.\begin{aligned} \eta_z &= \frac{1}{2\sqrt{\mu}} \left(\sqrt[3]{1 + \sqrt{1 + \frac{1}{27\,\mu}}} + \sqrt[3]{1 - \sqrt{1 + \frac{1}{27\,\mu}}} \right) \\ \eta_{st} &= \frac{1}{\sqrt{\mu}} \left(\sqrt[3]{1 + \sqrt{1 + \frac{8}{27\,\mu}}} + \sqrt[3]{1 - \sqrt{1 + \frac{8}{27\,\mu}}} \right) \end{aligned}\right\} \tag{35}$$

consider the effect of the nonlinearity on the maximum dynamic and the maximum static displacements, respectively. In the equations (35),

$$\mu = \frac{\alpha}{2} \left(\frac{z^0_{max}}{\lambda_0} \right)^2 = 2\alpha \left(\frac{q}{\lambda_0^3} \right)^2 \tag{36}$$

is the dimensionless parameter of nonlinearity. The dynamic factor

$$K_d = \frac{z_{max}}{z_{st}} = \frac{\sqrt[3]{1 + \sqrt{1 + 1/27\,\mu}} + \sqrt[3]{1 - \sqrt{1 + 1/27\,\mu}}}{\sqrt[3]{1 + \sqrt{1 + 8/27\,\mu}} + \sqrt[3]{1 - \sqrt{1 + 8/27\,\mu}}} \tag{37}$$

changes from $K_d = 2$ in the case of a linear system ($\mu = 0$) to $K_d = 1$ for a strongly nonlinear system ($\mu \to \infty$). The factors η_z, η_{st}, and K_d are plotted in Fig. 3 as functions of the dimensionless parameter of nonlinearity μ. This figure indicates that dynamic nonlinear effects are substantially greater than the static effects, and that the nonlinear effects are greater in the case of a "weak" nonlinearity.

The initial accelerations of the board can be easily obtained from the equation (17) by simply putting the displacement z equal to zero:

$$\ddot{z}_0 = q = c\ddot{w}_c \tag{38}$$

Thus, the factor c, expressed by the formula (18), is, in effect, the ratio of the maximum

initial relative ("elastic") acceleration of the PCB to the acceleration of its contour. The distribution of the total (absolute) accelerations w_i over the PCB surface can be obtained on the basis of the first formula in (3):

$$\ddot{w}_i = \ddot{w}_c - w_1(x,y)\ddot{z}_0 = -[cw_1(x,y) - 1]\ddot{w}_c \tag{39}$$

As evident from this formula, the initial absolute acceleration $\ddot{w}_i$ is the maximum on the support contour (where $w_1 = 0$) and is the minimum at the center of the board (where $w_1 = 1$):

$$\ddot{w}_{i,min} = -(c - 1)\ddot{w}_c \tag{40}$$

In the case of a simply supported board of finite aspect ratio, when the coordinate function w_1 is expressed by (4), we have

$$\ddot{w}_i(x,y) = -\left[\frac{16}{\pi^2}\cos\frac{\pi x}{a}\cos\frac{\pi y}{b} - 1\right]\ddot{w}_c \tag{41}$$

This formula indicates that the initial absolute accelerations are negative within the rectangular

$$\frac{x}{a} = \frac{y}{b} = \frac{1}{\pi}\arccos\frac{\pi^2}{16} = 0.2884\ . \tag{42}$$

The minimum absolute acceleration is in the center of the board, and, in accordance with (40), is

$$\ddot{w}_{i,min} = -0.621\ \ddot{w}_c \tag{43}$$

In the case of a clamped, board, we obtain, using the coordinate function (6), that the initial negative accelerations occur within the rectangular

$$\frac{x}{a} = \frac{y}{b} = 0.3098\ , \tag{44}$$

and that the minimum acceleration is

$$\ddot{w}_{i,min} = -0.778\ \ddot{w}_c\ . \tag{45}$$

Thus, negative initial accelerations occupy a quite large area and their absolute maxima are comparable with the magnitude of the external acceleration. This is important to have in mind, particularly, when evaluating the strength of solder joints in the devices located in the inner portion of a PCB, on its "front" side, i.e. on the side of the direction of motion. At the first moments of shock loading, such joints can experience rather high tensile stresses. These stresses have a potential to be more dangerous than even larger compressive stresses that occur later, at the end of the first quarter-period of vibrations.

In elongated boards, the region of negative initial accelerations is $-0.212\ a \le x \le 0.212\ a$ for a simply supported board, and $-0.169\ a \le x \le 0.169\ a$ for a clamped board. The initial accelerations at the center of the board are $\ddot{w}_{i,min} = -0.273\ \ddot{w}_c$ and $\ddot{w}_{i,min} = -0.297\ \ddot{w}_c$, respectively.

As one can see from the equations (17) and (29), the induced relative accelerations of the board become zero, when its displacement z becomes equal to its static value z_{st}. At this moment of time all the points of the board have the same acceleration as the support contour.

At the end of the first quarter-period of vibrations, when the board reaches its maximum deflection $z = z_{max}$, its relative ("elastic") acceleration, as follows from (17), is

$$\ddot{z}_{max} = q - \lambda_0^2 z_{max} - \alpha z_{max}^3 , \tag{46}$$

or, considering (28),

$$\ddot{z}_{max} = \lambda_0^2 z_{max} - 3q . \tag{47}$$

From (33) and (47) we find that the relative linear acceleration is

$$\ddot{z}^0_{max} = - q , \tag{48}$$

i.e. equal in magnitude and opposite in sign to the initial acceleration, expressed by (38). The formulas (47) and (48) indicate that the factor

$$\eta_{\ddot{z}} = \frac{\ddot{z}_{max}}{\ddot{z}^0_{max}} = 3 - \frac{\lambda_0^2 z_{max}}{q} = 3 - 2\eta_z \tag{49}$$

accounts for the effect of the nonlinearity on the maximum relative acceleration. This factor is plotted in Fig. 3. In a strongly nonlinear system ($\mu \to \infty$) the factor η_z, reflecting the effect of the nonlinearity on the maximum deflection is very (because the small nonlinear deflections). Therefore in such an extreme case the relative nonlinear acceleration can exceed the linear acceleration by up to a factor of 3.

Introduce a new dimensionless parameter δ, which will be used hereafter, so that

$$\mu = \frac{\alpha}{2}\left[\frac{z^0_{max}}{\lambda_0}\right]^2 = 4\,\frac{\delta^2 - 1}{(3 - \delta^2)^3} \tag{50}$$

The factor $\eta_{\ddot{z}}$ is equal to δ^2. Indeed, in this case the equation (49) yields: $\eta_z = \frac{3-\delta^2}{2}$, and the formula (50) results in the following equation for the factor η_z:

$$1 - \eta_z - \mu\eta_z^3 = 0 .$$

Since, as follows from (31) and (33), $\eta_z = \frac{\lambda_0^2 z_{max}}{2q}$, the above cubic equation leads to the equation (28). The calculated δ values are shown in Fig. 3 along with the μ values. When μ changes from zero to infinity, the δ value changes from 1 to $\sqrt{3}$.

The absolute (total) accelerations of the board at the moment of time equal to the quarter-period of vibrations are

$$\ddot{w}_{max} = \ddot{w}_c - w_1(x,y)\ddot{z}_{max} = \left[1 + c\eta_{\ddot{z}} w_1(x,y)\right]\ddot{w}_c \tag{51}$$

As evident from this formula, the directions of the maximum accelerations for all the points of the board coincide at this moment of time with the direction of the acceleration of the support contour. At the center of the board the absolute accelerations are by a factor of

$$\eta_0 = 1 + c\eta_{\ddot{z}}$$

greater than the acceleration of the support contour. In a linear system ($\eta_{\ddot{z}} = 1$) this factor is $\eta_0 = 1+c = 2.621$ for a finite aspect ratio simply supported board, $\eta_0 = 2.273$ for an elongated simply supported board, $\eta_0 = 2.778$ for a finite aspect ratio clamped board, and $\eta_0 = 2.165$ for an elongated clamped board. In strongly nonlinear systems, with the factor $\eta_{\ddot{z}}$ approaching 3, the factor η_0 of the total acceleration at the center of the board reaches $\eta_0 = 5.863$ in the case of a finite aspect ratio simply supported board, $\eta_0 = 4.819$ in the case of an elongated simply supported board, $\eta_0 = 6.334$ in the case of a finite aspect ratio clamped board, and $\eta_0 = 4.495$ in the case of an elongated clamped board. Thus, nonlinearity can result in a significant increase in the total (absolute) acceleration of the PCB. Clearly, at this moment of time the interconnections in the devices mounted on the "front" side of the board experience compressive stresses, while the interconnections on its "back" side are subjected to tension. It should be pointed out that because of the structural damping, the induced vibrations fade in the course of time, and therefore at the moments of time sufficiently remote from the moment of loading, the PCB accelerations are not different from the external acceleration $\ddot{w}_c$.

3.2. Solution to the equation of motion

In the previous section, the maxima of the PCB deflections, velocity, and acceleration were determined on the basis of more or less elementary considerations, without solving the equation of motion (17). This solution, i.e. the expression for the displacement of the board as a function of time, can be presented, using the relationship (27) in the form:

$$t = \int_0^z \frac{dz}{\sqrt{2qz - \lambda^2 z^2 - \frac{1}{2}\alpha z^4}} = \frac{u}{\sigma}, \tag{52}$$

where

$$u = F(\theta,k) = \int_0^\theta \frac{d\theta}{\sqrt{1 - k^2\sin^2\theta}} \tag{53}$$

is an elliptic integral of the first kind (see, for instance, [Reference 35,36]), k is the modulus of the elliptic function, $\theta = cnu$ is the amplitude of this function, and σ is the frequency parameter.

In order to express the parameters k and σ through the characteristics of the dynamic system (17), we seek the inversion of the integral (52) in the form:

$$z = z_{max} \frac{1 - cnu}{\delta + 1 + (\delta - 1)cnu} . \tag{54}$$

Here z_{max} is the maximum displacement, cnu is the elliptic cosine, and δ is a thus far unknown parameter of nonlinearity. Using the rules of differentiation of the elliptic functions [Reference 35,36] we obtain:

$$\dot{z} = 2\delta\sigma z_{max} \frac{snu\ dnu}{[\delta + 1 + (\delta - 1)cnu]^2} , \tag{55}$$

$$\ddot{z} = 2\delta\sigma^2 z_{max} \frac{(\delta + 1)(1 - 2k^2 sn^2 u)cnu + (\delta - 1)[1 + (1 - 2k^2)sn^2 u]}{[\delta + 1 + (\delta - 1)cnu]^3} , \tag{56}$$

where snu is the elliptic sine, and $dnu = \sqrt{1 - k^2 sn^2 u}$ is the function of delta-amplitude. After substituting (54) and (56) into (17), we conclude that the latter equation eise fulfilled, if the maximum displacement z_{max} is expressed by the equation (28), and the parameters k and σ are expressed by the formulas

$$k = \sqrt{\frac{(\delta - 1)(3 - \delta)}{8\delta}} , \sigma = \lambda_0 \sqrt{\frac{2\delta}{3 - \delta^2}} . \tag{57}$$

Here the parameter

$$\delta = \sqrt{1 + \frac{\alpha}{2q} z_{max}^3} = \sqrt{3 - \frac{\lambda_0^2}{q} z_{max}} = \sqrt{3 - 2\eta_z} \tag{58}$$

is related to the dimensionless parameter of nonlinearity μ, used earlier, by the equation (50). In the linear case ($\alpha = 0$), $\delta = 1$, $k = 0$, and $\sigma = \lambda_0$. In an opposite, strongly nonlinear, case ($\alpha \to \infty$), $z_{max} = 0$, $\delta = \sqrt{3}$, $k = \frac{1}{2}\sqrt{2 - \sqrt{3}} = 0.259$, and $\sigma \to \infty$. The elliptic functions, entering the formulas (54), (55), and (56), can be easily computed by using, for instance, a procedure suggested in [Reference 37].

The formula for the amplitude θ of the elliptic function can be obtained from (54), assuming $cnu = \cos\theta$. This results in the equation

$$\theta = \text{arccotan} \sqrt{\frac{1}{\delta}\left[\frac{z_{max}}{z} - 1\right]} . \tag{59}$$

The amplitude θ reaches its maximum value $\theta_{max} = \frac{\pi}{2}$, when the displacement z reaches z_{max}. In this case the integral (53) becomes complete elliptic integral of the first kind:

$$K(k) = F(\frac{\pi}{2}, k) = \int_0^{\pi/2} \frac{d\theta}{\sqrt{1 - k^2 \sin^2\theta}} . \tag{60}$$

Since the time required for the angle θ to change from zero to $\frac{\pi}{2}$ is equal to the quarter

of the period of vibrations, we conclude, on the basis of the solution (52), that this period should be $4\,\frac{K(k)}{\sigma}$. Hence, the frequency of the nonlinear vibrations of the PCB is

$$\omega = \frac{\pi\sigma}{2K(k)} \,. \tag{61}$$

In the linear case, $k = 0$, $K(0) = \frac{\pi}{2}$, $\delta = 1$, and $\omega = \sigma = \lambda_0$.

As follows from the obtained results, the effect of the nonlinearity on the maximum relative displacement, velocity, acceleration, and frequency of vibrations can be characterized by the factors:

$$\eta_z = \frac{3 - \delta^2}{2}, \quad \eta_{\ddot{z}} = \sqrt{\frac{1}{2}\eta_{st}(3 - \eta_{st})}, \quad \eta_{\ddot{z}} = \delta^2 \,, \tag{62}$$

$$\eta_\omega = \frac{\pi}{2K(k)}\,\frac{\sigma}{\lambda_0} = \frac{\pi}{2K(k)}\sqrt{\frac{2\delta}{3 - \delta^2}} \,. \tag{63}$$

4. Repetitive Instantaneous Impacts

In the case of repetitive impacts we use the equation (20), and seek the steady-state solution to this equation in the form:

$$z = A\frac{P}{M\lambda_0}\,\mathrm{cn}(\sigma t + \varepsilon, k) = A\frac{P}{M\lambda_0}\,\mathrm{cnu} \,, \tag{64}$$

where ε is the initial phase angle, A is the dimensionless amplitude (the ratio of the actual nonlinear amplitude to the amplitude $P/M\lambda_0$ of linear vibrations due to a single impulse of the magnitude P), k is the modulus of the elliptic function, and σ is the frequency parameter. From (64), by differentiation, we find:

$$\dot{z} = -A\frac{P}{M\lambda_0}\,\sigma\,\mathrm{snu\,dnu} \,, \tag{65}$$

$$\ddot{z} = A\frac{P}{M\lambda_0}\,\sigma^2\,\mathrm{cnu}\,(1 - 2k^2\mathrm{sn}^2 u) \,. \tag{66}$$

After substituting (64) and (66) into (20), we conclude that the relationship (64) is indeed the solution to the equation (20), if the parameters k and σ are related to the dimensionless amplitude A by the formulas:

$$\left.\begin{aligned} k &= \sqrt{\frac{\bar{\alpha}A^2}{2(1 + \bar{\alpha}A^2)}}\,, \\ \sigma &= \lambda_0\sqrt{1 + \bar{\alpha}A^2} = \frac{\lambda_0}{\sqrt{1 - 2k^2}}\,, \end{aligned}\right\} \tag{67}$$

where

$$\bar{\alpha} = \alpha \left(\frac{P}{M\lambda_0^2} \right)^2 = \alpha \left[c \frac{\dot{w}_c}{\lambda_0^2} \right]^2 \tag{68}$$

is the dimensionless parameter of nonlinearity, similar to the parameter μ used in the case of a suddenly applied constant acceleration. In the formula (68) the factor c is expressed by (18).

The dimensionless amplitude A and the initial phase angle ε can be determined on the basis of the following conditions of periodicity of the PCB vibrations:

$$z(0) = z(T_s), \quad \dot{z}(0) = \dot{z}(T_s) + \frac{P}{M} \tag{69}$$

The first condition reflects an assumption that the duration of the impact is so small that the displacement z remains unchanged during the time of the impact. The second condition indicates that the velocity of the system suddenly changes by the amount $\frac{P}{M}$, i.e. the system gains a momentum equal to the magnitude of the external impulse P.

Substituting the formulas (64) and (65) into the conditions (69), we obtain the following equations for the unknowns A and ε:

$$\left.\begin{aligned} cn(\varepsilon,k) &= cn(\sigma T_s + \varepsilon, k) \\ -\, sn(\varepsilon,k)\,dn(\varepsilon,k) &= sn(\sigma T_s + \varepsilon, k)\,dn(\sigma T_s + \varepsilon, k) + \frac{\lambda_0}{A\sigma} \end{aligned}\right\} \tag{70}$$

The first equation in (70) yields:

$$sn(\sigma T_s + 2\varepsilon, k) = 0, \quad cn(\sigma T_s + 2\varepsilon, k) = 1 ,$$

so that the amplitude of the elliptic function is

$$\theta = am(\sigma T_s + 2\varepsilon, k) = 2\pi i, \; i = 0, \pm 1, \pm 2, \ldots$$

and therefore

$$\sigma T_s + 2\varepsilon = \int_0^{2\pi i} \frac{d\theta}{\sqrt{1 - k^2 \sin^2\theta}} = 4iK(k) ,$$

where K(k) is the complete elliptic integral. Then the initial phase angle ε is

$$\varepsilon = 2iK(k) - \frac{1}{2}\sigma T_s, \quad i = 0, \pm 1, \pm 2, \ldots \tag{71}$$

The second equation in (70) can be rewritten, considering the first equation, as follows:

$$A = \frac{\lambda_0}{2\sigma F} , \tag{72}$$

where the function F is

$$F = |sn(\varepsilon,k)dn(\varepsilon,k)| = |sn(\varepsilon,k)\sqrt{1 - k^2 sn^2(\varepsilon,k)}| \tag{73}$$

After introducing the formula for σ from (67) into (72) and solving the obtained equation for the dimensionless amplitude A, we find:

$$A = \sqrt{\frac{\sqrt{1 + \bar{\alpha}/F^2} - 1}{2\bar{\alpha}}} \tag{74}$$

The vibration frequency can be evaluated by the formula (61), where, however, the parameters k and σ are expressed by (67).

In the case of linear vibrations ($\bar{\alpha} = 0$), we have: $k = 0$, $K(0) = \frac{\pi}{2}$, $\omega = \sigma = \lambda_0$, $\varepsilon = i\pi - \frac{1}{2}\lambda_0 T_s$, $sn(\varepsilon,0) = \sin\varepsilon = -\sin\frac{\lambda_0 T_s}{2}$, $dn(\varepsilon,0) = 1$, and $F = |\sin\frac{\lambda_0 T_s}{2}|$
Then the formula (74) yields:

$$A = \lim_{\bar{\alpha}\to 0}\sqrt{\frac{\sqrt{1 + \bar{\alpha}/F^2} - 1}{2\bar{\alpha}}} = \frac{1}{2F}$$

$$= \frac{1}{2}\left|\operatorname{cosec}\frac{\lambda_0 T_s}{2}\right| . \tag{75}$$

This formula was obtained first by Duffing [Reference 10].

In the case of a single impulse, the conditions of periodicity (69) should be replaced by the initial conditions

$$z(0) = 0, \dot{z}(0) = \frac{P}{M} ,$$

and the initial phase angle ε should be put equal to zero. Then the dimensionless vibration amplitude becomes

$$A_1 = \sqrt{\frac{\sqrt{1 + 2\bar{\alpha}} - 1}{\bar{\alpha}}} \tag{76}$$

Clearly, the amplitude of the shock-excited vibrations, expressed by (74), is minimum when $F = F_{max}$. From (73), considering that $sn^2\, u \le 1$, we find:

$$F_{max}^2 = 1 - k^2 = \frac{1 + \sqrt{1 + \bar{\alpha}/2}}{2\sqrt{1 + \bar{\alpha}/2}} \tag{77}$$

This results in the following formula for the minimum amplitude:

$$A_{min} = \sqrt{\frac{\sqrt{1 + \bar{\alpha}/2} - 1}{\bar{\alpha}}} \quad . \tag{78}$$

The amplitudes of the vibrations due to repetitive impacts can be computed as a function of the excitation frequency $\lambda_s = 2\pi/T_s$ using the following procedure:

1. For the given PCB, determine the generalized masses M_0 and M, the linear frequency λ_0, and the parameter of nonlinearity α, using the formulas obtained in Section 2.

2. For the given "step" $\dot{w}_c$ in the contour velocity, calculate the dimensionless parameter $\bar{\alpha}$ of nonlinearity by (68), and the F^2_{max} value by (77).

3. For the F^2 values within the range $0 \le F^2 \le F^2_{max}$, compute the dimensionless amplitude *A* by (74) and the corresponding k^2 value by the first formula in (67).

4. For each k^2, starting with [Reference 36]

$$a_0 = 1, \quad b_0 = \sqrt{1 - k^2}, \quad \phi_0 = \arcsin \sqrt{1 - \frac{\sqrt{1 - 4k^2F^2}}{2k^2}} \quad ,$$

compute

$$a_{r+1} = \frac{a_r + b_r}{2}, \quad b_{r+1} = \sqrt{a_r b_r}, \quad c_r = \sqrt{a_r^2 - b_r^2}, \quad r = 0,1,2,...$$

and

$$\phi_r = \arcsin \left[\frac{\sin 2\phi_{r-1}}{\sqrt{1 + \frac{c_r^2}{a_r^2} + 2\frac{c_r}{a_r} \cos 2\phi_{r-1}}} \right], \quad r = 1,2,...$$

The iterations should be stopped at $r = N$, when $c_r \approx 0$. Then determine $\ell = a_N = b_N$, and $n = \phi_{N-1}$.

5. For each amplitude A, calculate the frequency

$$\omega = \lambda_0 \ell \sqrt{1 + \bar{\alpha} A^2}$$

of nonlinear vibrations and the linear frequency ratios

$$\left[\frac{\lambda_0}{\lambda_s}\right]_i = \frac{\lambda_0}{\omega} \left| i + \frac{n}{\pi} 2^{1-N} \right| , \quad i = 0, \pm 1, \pm .2,...$$

For sufficiently large λ_0/λ_s ratios, i.e. for large i values, this formula can be simplified:

$$\left[\frac{\lambda_0}{\lambda_s}\right]_i = i\,\frac{\lambda_0}{\omega}\,,\quad i = 0, \pm 1, \pm 2,\ldots$$

The maximum acceleration, in accordance with (66), is

$$\ddot{z}_{max} = A\,\frac{P}{M\lambda_0}\,\sigma^2 = \eta_{\ddot{z}}\,\frac{P\lambda_0}{M}\,, \tag{79}$$

where the factor

$$\eta_{\ddot{z}} = A\,(1 + \bar{\alpha}A^2) \tag{80}$$

reflects the effects of the vibrations nonlinearity and the periodicity of the impacts. Note that if the ratios $\frac{\lambda_0}{\lambda_s}$ of the linear natural frequency to the frequency of excitation are large, the vibrations can become "stochastically unstable" i.e. the system can oscillate in a random-like manner despite the non-random excitation [Reference 22,38].

5. Stresses

The dynamic stresses in the PCB can be calculated on the basis of the formulas [Reference 5,6]:

$$\left.\begin{aligned}
\sigma_x &= \sigma_x^0 = \frac{6D}{h^2}\left(\frac{\partial^2 w}{\partial x^2} + \nu\frac{\partial^2 w}{\partial y^2}\right)\\
\sigma_y &= \sigma_y^0 - \frac{6D}{h^2}\left(\frac{\partial^2 w}{\partial y^2} + \nu\frac{\partial^2 w}{\partial x^2}\right)\\
\tau_{xy} &= \tau_{xy}^0 - \frac{6D}{h^2}(1-\nu)\frac{\partial^2 w}{\partial x\partial y}
\end{aligned}\right\},$$

where the first terms are the "membrane" stresses, expressed through the stress function ϕ as

$$\sigma_x^0 = \frac{\partial^2\phi}{\partial y^2}\,,\ \sigma_y^0 = \frac{\partial^2\phi}{\partial x^2}\,,\ \tau_{xy}^0 = -\frac{\partial^2\phi}{\partial x\partial y}\,,$$

and the second terms are due to bending. Using the equations (3), and the appropriate formulas for the coordinate function and static stress function, we find that the maximum normal stresses in a simply supported board of finite aspect ratio occur at its center ($x = y = 0$) and are as follows:

$$\left.\begin{aligned}\sigma_x &= \frac{\pi^2 E h^2}{2a^2 b^2}\,\frac{\nu a^2 + b^2}{1-\nu^2}\,\zeta\left[1 + \frac{\nu a^2 + (2-\nu^2)b^2}{4(\nu a^2 + b^2)}\zeta\right] \\ \sigma_y &= \frac{\pi^2 E h^2}{2a^2 b^2}\,\frac{a^2 + \nu b^2}{1-\nu^2}\,\zeta\left[1 + \frac{(2-\nu^2)a^2 + \nu b^2}{4(a^2 + \nu b^2)}\zeta\right].\end{aligned}\right\} \tag{81}$$

Here ζ is the dimensionless maximum displacement, which is equal to $\zeta = \frac{z_{max}}{h}$ in the case of a suddenly applied acceleration, and to $\zeta = A\frac{P}{M\lambda_0 h}$ in the case of repetitive impacts. The maximum shearing stress occurs along the rectangular $x = \pm \frac{a}{2}$, $y = \pm \frac{b}{2}$, and is

$$\tau_{xy} = \frac{\pi^2 G h^2}{ab}\zeta\,, \tag{82}$$

where $G = \frac{E}{2(1+\nu)}$ is the shear modulus of the material. In a special case of a square board ($a = b$):

$$\left.\begin{aligned}\sigma_x = \sigma_y &= \frac{\pi^2 E}{2(1-\nu)}\left(\frac{h}{a}\right)^2 \zeta\left[1 + \frac{2-\nu}{4}\zeta\right] \\ \tau_{xy} &= \pi^2 G\left(\frac{h}{a}\right)^2 \zeta\end{aligned}\right\} \tag{83}$$

In the case of an elongated board ($b \to \infty$), the shearing stress is zero, and the maximum normal stress, calculated on the basis of the equation (8), is

$$\sigma_x = \frac{\pi^2 E}{2(1-\nu^2)}\left(\frac{h}{a}\right)^2 \zeta\left[1 + \frac{\zeta}{2}\right] \tag{84}$$

In the case of a clamped board, the normal stresses at the center of the board are:

$$\left.\begin{aligned}
\sigma_x &= \frac{\pi^2 E h^2}{a^2 b^2}\,\frac{\nu a^2 + b^2}{1-\nu^2}\,\zeta\left\{1 + \frac{1-\nu^2}{32}\,\frac{b^2}{\nu a^2 + b^2}\,\zeta\right. \\
&\times\left[5 + \frac{3}{1-\nu^2}\left(1 + \nu\frac{a^2}{b^2}\right) + \frac{8a^2b^2}{(a^2+b^2)^2} + \right. \\
&\left.\left. + \frac{16a^2b^2}{(4a^2+b^2)^2} + \frac{4a^2b^2}{(a^2+4b^2)^2}\right]\right\}, \\
\sigma_y &= \frac{\pi^2 E h^2}{a^2 b^2}\,\frac{a^2 + \nu b^2}{1-\nu^2}\,\zeta\left\{1 + \frac{1-\nu^2}{32}\,\frac{a^2}{a^2 + \nu b^2}\,\zeta\right. \\
&\times\left[5 + \frac{3}{1-\nu^2}\left(1 + \nu\frac{b^2}{a^2}\right) + \frac{8a^2b^2}{(a^2+b^2)^2} + \right. \\
&\left.\left. + \frac{4a^2b^2}{(4a^2+b^2)^2} + \frac{16a^2b^2}{(a^2+4b^2)^2}\right]\right\}
\end{aligned}\right\} \tag{85}$$

The maximum shearing stress occurs along the perimeter of the rectangular $x = \pm\frac{a}{4}$, $y = \pm\frac{b}{4}$ and is

$$\tau_{xy} = \frac{\pi^2 G h^2}{ab}\,\zeta\left[1 + \frac{1+\nu}{2}\,\frac{a^2b^2}{(a^2+b^2)^2}\,\zeta\right] \tag{86}$$

In the case of a square board ($a = b$)

$$\left.\begin{aligned}
\sigma_x = \sigma_y &= \frac{\pi^2 E}{1-\nu}\left(\frac{h}{a}\right)^2 \zeta\left[1 + \frac{3(18-13\nu)}{160}\,\zeta\right] \\
\tau_{xy} &= \pi^2 G\left(\frac{h}{a}\right)^2 \zeta\left(1 + \frac{1+\nu}{8}\,\zeta\right)
\end{aligned}\right\} \tag{87}$$

The maximum normal stress in an elongated clamped board is

$$\sigma_x \cong 16 \frac{E}{1-\nu^2} \left(\frac{h}{a}\right)^2 \zeta(1 + 0.193\zeta) \tag{88}$$

NUMERICAL EXAMPLES

1. Let an ASTM/NEMA Class G-10 fiber glass PCB, simply supported on its contour, experiences constant suddenly applied acceleration $\ddot{w}_c = 25g$ acting on its contour. Let the weight of all the surface mounted components be, say, 20% of the board's weight, and let there be a certain flexibility in the spot where the given surface mounted device can be mounted on the board. Let this device be able to withstand accelerations not exceeding, say, 100g. The purpose of the calculation below is to determine the PCB area where the device can be safely installed, so that its strength and the reliable operation are not compromised. We use the following input data: PCB material density $\rho = 1.8 g/cm^3$, Young's modulus $E = 17.2 \times 10^4$ kgf/cm^2, Poisson's ratio $\nu = 0.3$, ultimate strength in tension $\sigma_u \cong 2500$ kgf/cm^2, thickness $h = 0.159$ cm, and the in-plane dimensions are $a = 20.3$cm and $b = 30.5$cm (the aspect ratio $b/a = 1.5$).

Using the formulas (21), we find that the linear frequency of free vibrations of the board is $\lambda_0 = 463.5 sec^{-1}$, and the parameter of nonlinearity is $\alpha = 12.3 \times 10^6$ cm^{-2} sec^{-2}. The excitation force acting on the PCB contour, in accordance with the formula $q = c\ddot{w}_c$, where the parameter c is expressed by (18), is $q = 1.621 \times 25g = 39715 cm/sec^2$. The maximum linear dynamic displacement, determined by (33), is $z^0_{max} = 2q/\lambda_0^2 = 0.370$cm, which is more than twice as large as the PCB's thickness. The dimensionless parameter of nonlinearity given by (36), is $\mu = \frac{1}{2} \alpha (z^0_{max}/\lambda_0)^2 = 3.905$. Then, using the first formula in (35), we find that the factor considering the effect of the nonlinearity on the maximum deflection is $\eta_z = 0.347$, so that this deflection is $z_{max} = \eta_z z^0_{max} = 0.128$cm, which is only 80% of the board thickness. The factor accounting for the effect of the nonlinearity in the maximum induced acceleration can be determined on the basis of the formula (49) and is $\eta_{\ddot{z}} = 3 - 2\eta_z = 2.306$. Thus, the nonlinear (actual) acceleration is substantially larger than the acceleration predicted using linear approach. The distribution of the total (absolute) maximum (in time) accelerations over the board's surface, as given by (51), is

$$\ddot{w}_{max} = 25g \left[1 + 3.738 \cos\frac{\pi x}{a} \cos\frac{\pi y}{b}\right]$$

The condition $\ddot{w}_{max} \leq 100g$ results in the following equation of the rectangular restricting the region where the device can be safely mounted (Fig. 4):

$$\cos\frac{\pi x}{a} \cos\frac{\pi y}{b} = 0.803 \ .$$

Thus, the device should be mounted, for safe operation, outside the region

$$\frac{x}{a} = \frac{y}{b} = \pm 0.203 \ .$$

The maximum stresses, computed in accordance with the equations (81) and (82), are $\sigma_x = 71.1\text{kgf/cm}^2$, $\sigma_y = 44.9\text{kgf/cm}^2$, and $\tau_{xy} = 21.5\text{kgf/cm}^2$. These values are very low compared to the ultimate stress $\sigma_a = 2500\text{kgf/cm}^2$.

The calculated maximum acceleration at the center of the board is $\ddot{w}_{max} = 118.45\text{g}$. Note that the linear approach would result in the following maximum acceleration at the center of PCB:

$$\ddot{w}_{max} = (1 + c)\ddot{w}_c = 2.621\ddot{w}_c = 65.5\text{g} ,$$

and would lead to an erroneous conclusion that the device could be safely mounted throughout the board.

2. Examine now an elongated simply supported PCB made of the same material as in the previous example and subjected to periodic instantaneous impulsive loads, characterized by a velocity step of 0.5m/sec.

The mass of the board per unit area is $m = 1.2\rho h = 0.3456\text{g/cm}^2$ and its flexural rigidity is $D = 64.5\text{kgfcm}$. Then the formulas (22) yield: $\lambda_0 = 320.9$ 1/sec, $\alpha = 12.2 \times 10^6\ \text{cm}^{-2}\ \text{sec}^{-2}$. The dimensionless parameter of nonlinearity defined by (68), is $\bar{\alpha} = 4.664$. Then the formula (76) results in the following value of the dimensionless amplitude of nonlinear vibrations due to a single impact: $A_1 = 0.689$. Hence, the amplitude of nonlinear vibrations caused by a single impact is by a factor of 0.689 smaller than the amplitude $A_1 = c\frac{\dot{w}_c}{\lambda_0} = 0.198\text{cm}$ *of linear vibrations*, caused by such an impact, i.e. is only 0.136 cm.

The parameter F_{max}, defined by (77), is $F^2_{max} = 0.7739$, and the minimum dimensionless amplitude of the vibrations caused by periodic impacts is, as predicted by (78), $A_{min} = 0.4207$. Hence, for the most favorable ratio of the natural and excitation frequencies, the amplitude of the nonlinear vibrations due to repetitive impacts is by a factor of 0.4207 smaller than the amplitude of linear vibrations due to a single impulse of the same magnitude.

The calculations of the induced displacements, accelerations, and dynamic stresses are carried out in the Table 1. As evident from this table, the induced stresses are very low, while the induced accelerations can exceed significantly the accelerations due to a single impact. The calculated response functions for the maximum accelerations $\ddot{z}_{max}$ are plotted in Fig. 5, where the ratios $\ddot{z}_{max}/g$ are presented versus the ratios λ_s/λ_0 of the excitation to the natural frequency. As evident from the obtained data, the linear and nonlinear responses are substantially different, and nonlinear accelerations can exceed considerably the linear ones. If, for instance, the frequency of the impacts is such that the ratio λ_s/λ_0 is 0.85, then the nonlinear accelerations are by a factor of 2.2 larger than the linear accelerations. On the other hand, since nonlinearity "destroys resonances" (see, for instance, [Reference 38]), the maximum accelerations in a nonlinear shock-excited system can never be as large as in a linear system at resonant or close-to-resonant conditions. Let, for instance, the frequency ratio in the example in question be close to 0.5 and let the given electronic component be unable to withstand accelerations higher than, say, 50g. As follows from Fig. 5, mounting of such a component can be permitted, since the actual (nonlinear) accelerations never exceed 40g. A linear approach, however,

can result in an erroneous conclusion that the installation of this component should not be allowed. In this connection we would like to point out that if the actual PCB support conditions are such that the supports can draw closer during the board's vibrations (i.e. if the system is linear indeed), then at resonant conditions such a PCB can impose substantially higher accelerations on the surface-mounted components, then a board with an immovable contour. Therefore, if the resonant frequencies cannot be avoided and/or predicted with sufficient accuracy, then fixing of the PCB support contour can be regarded as a feasible design measure, aimed at the "destruction" of linear resonance conditions. Obviously, this may not be necessary in the case of strong damping, which would keep even resonance amplitudes at a sufficiently low level.

CONCLUSIONS

The following major conclusions can be drawn from the performed analysis.

- Simple and easy-to-apply analytical models have been developed for the predictions of the nonlinear dynamic response of a flexible PCB to constant accelerations or repetitive impacts, applied to its support contour.

- In the case of large PCB deflections and immovable contour, it is important to account for the nonlinearity of the vibrations.

- The obtained results can be used to predict the accelerations experienced by electronic components and devices, surface mounted on flexible printed circuit boards, as well as when choosing the appropriate PCB type and dimensions and the most rational lay-out of the components on the board.

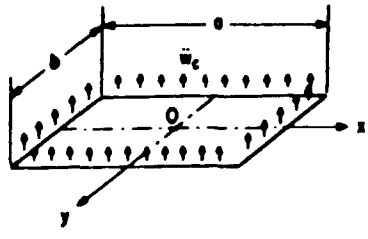


FIGURE 1

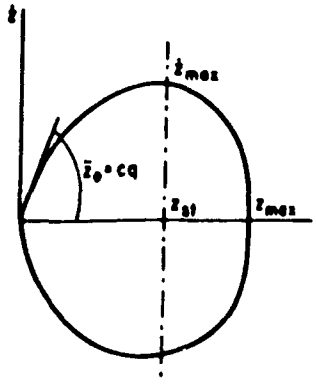


FIGURE 2

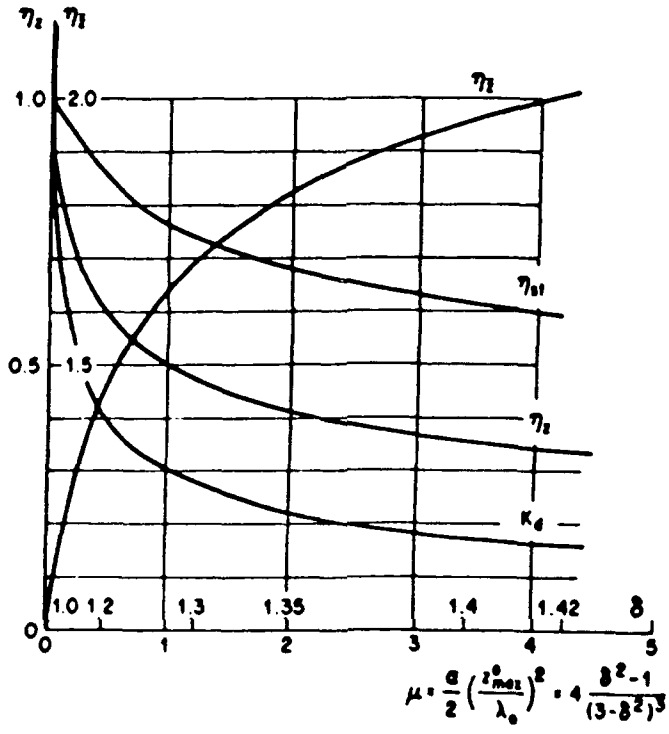


FIGURE 3

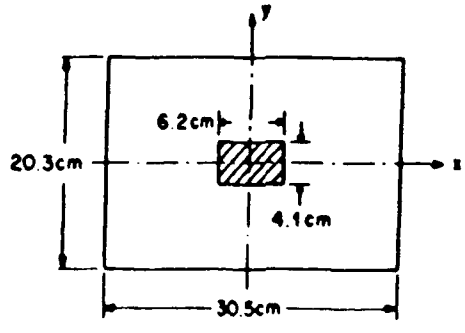
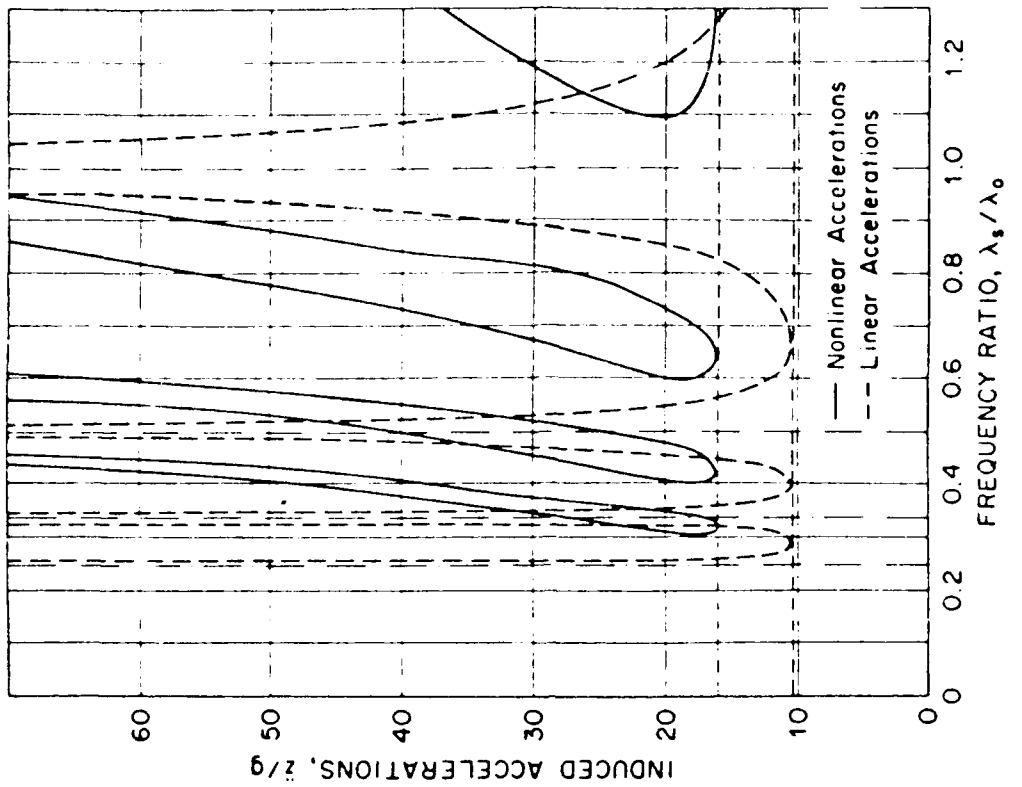


FIGURE 4



$\delta = 4.664$, $\lambda_o = 3209\ \text{sec}^{-1}$

j	0	01	02	04	06	07	075	07239
λ^j	–	0.16327	0.4215	0.2742	0.2103	0.1896	0.1809	0.1770
A_j	–	0.7954	0.6492	0.5237	0.4586	0.4194	0.4252	0.4207
b_j^2	0.5	0.1754	0.3314	0.2806	0.2476	0.2346	0.2287	0.2261
k	0.70071	0.6111	0.9757	0.9297	0.8976	0.8644	0.8783	0.8755
h_0	1	1	1	1	1	1	1	1
a_0	0.70711	0.7916	0.8177	0.8482	0.8674	0.8749	0.8782	0.8797
h_1	0.84515	0.8994	0.9088	0.9241	0.9337	0.9374	0.9191	0.9198
a_1	0.84852	0.8897	0.9043	0.9210	0.9319	0.9354	0.9171	0.9179
h_2	0.11461	0.11442	0.06065	0.07590	0.0663	0.0618	0.0609	0.0594
a_2	0.84172	0.8927	0.9065	0.9225	0.9325	0.9164	0.9381	0.9388
h_3	0.84172	0.8927	0.9065	0.9225	0.9325	0.9164	0.9381	0.9388
c_j	0	0	0	0	0	0	0	0
ℓ	0.8472	0.8927	0.9065	0.9225	0.9325	0.9164	0.9381	0.9388
N	2	2	2	2	2	2	2	2
Φ_0	0	0.1284	0.4826	0.7445	1.0278	1.2215	1.1730	1.1708
Φ_1	0	0.5918	0.8878	1.4078	1.1508	0.7432	0.4222	0
n	0	0.5918	0.8878	1.4078	1.1508	0.7432	0.4222	0
$\frac{n^2}{\pi^2}$	0	0.09419	0.14130	0.22406	0.18316	0.11828	0.06719	0
ω/λ_o	–	1.7744	1.5611	1.3926	1.3324	1.2854	1.2736	1.2684
n_o	–	3.1426	1.9254	1.1934	0.9084	0.8204	0.7837	0.7680
$\sigma_o \frac{\text{kgf}}{\text{cm}^2}$	–	8.0	6.51	4.96	4.21	3.95	3.84	3.79

$\frac{\lambda_s}{\lambda_o} = \frac{\omega}{\lambda_o} \left| 1 + \frac{n}{\pi} 2^{1/2} \right|^{-1}$, $\mu = 0, \pm 1, \pm 2, \ldots$

μ								
0	–	18.8385	11.0481	6.2153	7.1653	10.8674	18.9552	–
-1	–	1.9489	1.8180	1.7947	1.6067	1.4578	1.3653	1.2684
1	–	1.6217	1.3678	1.1377	1.1092	1.1494	1.1934	1.2684
-2	–	0.9310	0.8199	0.7841	0.7223	0.6831	0.6589	0.6342
2	–	0.8473	0.7290	0.6281	0.6011	0.6468	0.6161	0.6342
-3	–	0.6196	0.5461	0.5017	0.4659	0.4460	0.4343	0.4228
3	–	0.5735	0.4970	0.4319	0.4123	0.4122	0.4152	0.4228
4	–	0.4543	0.4046	0.3648	0.3418	0.3311	0.3258	0.3171
4	–	0.4134	0.3720	0.3297	0.3137	0.3121	0.3151	0.3171

FIGURE 5

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INFORMATION RETRIEVAL USING THE DATA ANALYSIS RESEARCH TOOL

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ABSTRACT

This paper will demonstrate a system that the Naval Weapons Center, China Lake, Electronic Production Technology Branch, is using to access electronic manufacturing specifications and technical documents. The Data Analysis Research Tool (DART) navigates through information quickly and easily.

"Knowledge is of two kinds," according to Samuel Johnson. "We know a subject ourselves or we know where we can find information upon it." DART is a system that allows users to "get-a-hold" of the information overload that is flooding the electronics industry. Furthermore, DART is low-cost, easy-to-use, and expandable.

INTRODUCTION

Imagine a personal device that would allow an individual to easily store up to 5,000 pages of new material a day. Books of all sorts, pictures, current periodicals, newspapers, etc. Imagine being able to retrieve any of that information in an instant. Imagine further the ability to instantly create permanent links between related information at the push of a button regardless of its date, format or source. Sound like some modern day marketing promise? Actually it's the remarkable vision of a man who called for nothing less than a new relationship between thinking man and the sum of our knowledge.

In 1945 Dr. Vannevar Bush, Franklin D. Roosevelt's Director of the Office of Scientific Research and Development, published a prophetic paper in *The Atlantic Monthly* entitled "As We May Think". This seminal paper was a call to arms for scientists to apply their energies toward new ways of preserving and manipulating the summation of human experience. He felt such an endeavor was most worthy of the post-war research and development community. "Presumably man's spirit should be elevated if he can better review his shady past and analyze more completely and objectively his present problems. He has built a civilization so complex that he needs to mechanize his records more fully if he is to push his experiment to its logical conclusion and not merely become bogged down part way there by overtaxing his limited memory. His excursions may be more enjoyable if he can reacquire the privilege of forgetting the manifold things he does not need to have immediately at hand, with some assurance that he can find them again if they prove important." (Reference 1). His words are more relevant in today's Information Age than when they were originally written.

Reading Dr. Bush's paper in 1991 is a humbling experience. It's easy to marvel at our modern day accomplishments, but in the context of his vision, we have barely progressed beyond the embryonic stage. While we have achieved most of the technology required to realize his vision, we have scarcely begun to provide the content necessary to make it meaningful. To truly revolutionize the way we think, learn, work and communicate, we must make our information more easily accessible, not just create more of it.

But let's take a closer look at his vision before we tackle the issue of content. Dr. Bush threw down the gauntlet when he declared, "The summation of human experience is being expanded at a prodigious rate, and the means we use for threading through the consequent maze to the momentarily important item is the same as was used in the days of square-rigged ships." (Reference 2). He went on to say, "The human mind operates by association...the process of tying two items together is the important thing." (Reference 3). The key therefore is to provide not only a huge repository for information but, more importantly, to provide a means for linking salient data to provide new insights.

Dr. Bush's paper sparked a new line of research that continues to this day. The first major work in the area was performed by Douglas C. Engelbart in 1962 at the Stanford Research Institute under joint sponsorship from the Institute and the Air Force Office of Scientific Research. The resulting paper, "*Augmenting Human Intellect: A Conceptual Framework*", laid the groundwork for today's commercial products. In his introduction Mr. Engelbart states the goals of his research quite clearly:

> "By 'augmenting human intellect' we mean increasing the capability of a man to approach a complex problem situation, to gain comprehension to suit his particular needs, and to derive solutions to problems. Increased capability in this respect is taken to mean a mixture of the following: more-rapid comprehension, better comprehension, the possibility of gaining a useful degree of comprehension in a situation that previously was too complex, speedier solutions, better solutions, and the possibility of finding solutions to problems that before seemed insoluble. And by 'complex situation' we include the professional problems of diplomats, executives, social scientists, life scientists, physical scientists, attorneys, designers--whether the problem situation exists for twenty minutes or twenty years. We do not speak of isolated clever tricks that help in particular situations. We refer to a way of life in an integrated domain where hunches, cut-and-try, intangibles, and the human 'feel for a situation' usefully co-exist with powerful concepts, streamlined terminology and notation, sophisticated methods, and high-powered electronic aids." (Reference 4)

Mr. Engelbart goes on to define a detailed and stunning blueprint for designing a computer based augmentation system.

In its current form, this area of research is now more commonly referred to as "hypermedia". This term is derived from the concept of "hypertext", a term coined by Ted Nelson in the mid-1960's. Mr. Nelson's early work built on the concepts laid out by Engelbart and Bush. He developed a computer system called Xanadu which was designed to use links to organize large bodies of online literature. He later went on to design the Hypertext Editing System at Brown University with Andy van Dam. (Reference 5).

Today, there are several commercial products and significant ongoing research projects that have their roots in these early works. The term "hypertext" has been expanded to "hypermedia" to accommodate additional data types such as graphics, sound, animation and video. This technology has also proven to be an excellent tool for controlling and integrating a multitude of information sources ranging in diversity from cable TV, VCR's, laserdisc players, and CD-ROM drives, to remote mainframe databases and information networks. Current research projects include NoteCards from Xerox Palo Alto Research Center, Neptune from Tektronix, Intermedia from Brown University and the Media Lab at MIT. Commercial products include HyperCard from Claris Corporation, ToolBook from Asymetrix, Plus from Spinnaker Software Corporation, and SuperCard from Aldus Corporation.

THE DATA ANALYSIS RESEARCH TOOL

STATEMENT OF NEED

"Knowledge, Samuel Johnson once wrote, "is of two kinds. We know a subject ourselves, or we know where we can find information upon it." Two centuries later, our body of knowledge has expanded in ways Johnson couldn't have imagined. Finding information is no longer that simple.

There is information everywhere: trade associations, universities, government agencies, corporations, think tanks, historical societies, nonprofit groups, and on and on. Any one may be the best repository of both historical and up-to-date information on a given subject. But tracking down the best sources-particularly those that are ready, willing, and able to help you-usually is time consuming. Even worse, such searches often are futile (Reference 6).

Information overload is one of the most serious handicaps facing today's business manager and government executive. In the Industrial Society the critical problems were the lack of information and the inability to retrieve it. Now, with access to so much information, the ability to make decisions and resolve conflicts is limited simply because so much time is spent going over all the pertinent and peripheral information bearing on every subject within the area of operation.

The manager in the information-intensive enterprise or government agency must determine what information he or she needs to know in order to act. Since information has a price tag, the cost of collecting all information on a specific subject must be carefully scrutinized. Nice-to-know information is not only costly, but may actually hinder the decision-making process. Need to know must be the primary guideline for effective managers (Reference 7).

The Electronics Production Technology Branch at the Naval Weapons Center, China Lake, deals with numerous military and industry specifications. Like most other companies or government agencies, the Branch is flooded with an over-abundance of information related to electronic production. Their need is simply to make accessible pertinent information electronically using an user-friendly computer interface. The need is being fulfilled through the Data Analysis Research Tool (DART).

PROJECT GOAL AND TECHNICAL OBJECTIVES

The goal of DART is to facilitate research into electronic production data. Intended end-users are quality assurance specialists, printed-wiring board manufacturers, and production managers. Currently, DART is used extensively by the Electronic Production Technology Branch quality assurance specialists and the Printed Wiring Board Shop technical managers. However, DART's usage is spreading to reliability personnel and upper management.

DART's function and scope is expandable and flexible to the environment. The technical objectives of DART are the following:

- Allow pertinent military specifications to be accessed via a computer network
- Link technical documentation or findings to related paragraphs within government specifications
- Provide comprehensive indexing of every word of every document entered into DART
- Print selected paragraphs to any printer or disk for electronic retrieval by any word processor
- Display any line drawing or photograph (Black & White, grayscale, or color)
- Display animation or video clips
- Play digitized sounds or voice
- Allow multiple users to access documents at the same time
- Control locked media such as videodiscs
- Access and interact with host data on a variety of minicomputer and mainframe systems in a uniform way, regardless of the particular host, operating system, database management system, or network connection

APPROACH AND EXPECTED BENEFITS

The Naval Weapons Center, China Lake, is predominantly a Macintosh community with an extensive network system. Most government workers are connected to a local area network through their Macintosh. The Data Analysis Research Tool took advantage of this situation by using existing off-the-shelf hardware and software.

HyperCard was selected as the development software for the DART project. The primary reason is that HyperCard has been included with every Macintosh since August 1987. Also, equally important:

- HyperCard's scripting language, HyperTalk, allows complete control over the user interface
- External Commands and External Functions extend HyperCard beyond its original capabilities
- Third-party software enhancements to HyperCard make it a very open development tool

The approached used to design DART is overtly simple. Documents are scanned and the text is converted to electronic text while the line drawings or photographs are converted to standard picture formats (i.e. PICT or TIFF). The information is then imported into a HyperCard program (called a stack). After putting the information into the stack, links are created from text to text, numbers to text, text to pictures, etc. Links allow the user to rapidly move from paragraph to paragraph to picture to specification to whatever. Once the information has been linked, an index is created from every word of every document. Finally, the completed stack is placed into a convenient entry point (called the Home stack) for users.

The following scenario will help to explain the simplicity and beauty behind the DART system. The computer user logs onto the network and selects the Data Analysis Research Tool file server. Then he/she opens up the Home stack. From the Home stack, the user scrolls up or down and selects any one of several specifications. By clicking on the desired specification, the user is taken to the complete document. From within the document, the user can call up the master index and search for any word or words. For example, searching for "solder" currently brings up 3,000 instances that the user can immediately go to. The search can be further refined by searching for all occurrences of the word "flux" that appear within 10 words or less of the word "solder".

Besides searching for information, the user can browse through the complete specification line-by-line. While going through the document, the user will notice that certain words are in italics. Words in italics indicate that there is additional amplification. For instance, in one of the paragraphs in MIL-STD-2000A, the word *capability* is in italics. Clicking on *capability* takes the user to another document explaining in detail the precise meaning of that word in that context. Also, clicking on any figure (i.e the word figure) brings up the respective picture. Finally, the user can print the document to a printer for a hard copy or to a disk for an electronic copy.

The number one design consideration behind DART, is that it be extremely user-friendly. The average person requires only 10-15 minutes of instruction before he/she can use DART proficiently. DART's premise is that people will actually use a computer program if the commands are intuitive and the learning curve is minimal.

DART promotes intelligent decision making. Instead of relying exquisitely on memory, the system takes the drudge work out of manually searching through countless specifications and technical documents. The benefits are faster retrieval of pertinent information and increased worker efficiency.

FUTURE GOALS

DART is a HyperCard based project using external commands and functions. These external commands and functions give HyperCard its "openness." By creating external commands and functions from conventional programming languages, HyperCard becomes a rich environment with near unlimited potential.

The future calls for continued growth in DART's baseline of documents using the existing Macintosh platform. But, the future also calls for porting the information to other platforms (i.e. Windows 3.0, OS/2, Unix).

DART's premier future goal, however, is to establish a nation-wide Soldering Technology repository of information. The information would be available via a modem or distributed via CD-ROM's. Nevertheless, funding will be the major obstacle. The technology is here, the need is here, the will is here, but unfortunately, our obsession with short-term results is also present. The organizations that will excel in the 1990's and beyond will be those that manage information as a major resource.

RETROSPECT

Our inability to grasp the concept is largely the results of information's intangible nature. It can be printed, spoken, drawn, and projected but these forms are mere representations of information. The marks on a page or screen, the sounds of speech and

music - none of this is information unless it conveys meaning to someone. Yet human history demonstrates a long-standing need for information and the skills you manipulate it (Reference 8).

If you've performed any kind of research, like preparing a term paper, you may have recognized that hardly any fact exists in a vacuum. For example, Julius Caesar was assassinated on March 15th in 44 B.C., yet it's difficult to consider that bit of information entirely on its own. You probably have other questions relating to the incident that require additional information: who were the assassins; what was their motivation; on what literature is the actual date based; what was the political and social climate of the time; what happened after the assassination?

The trouble is, if you find an information source for the event, that source likely won't have the additional information you require. You need to branch away from a strictly data-based collection of facts to other collections, such as information bases centered around literature of the time or historical observations made many centuries later. What this points to is that information very often consists of threads emanating in many threads running in yet other directions, and so on.

EVERYDAY LINKS

This phenomenon is best summed up in an excerpt from Alexander Solzhenitsyn's Cancer Ward:

"As every man goes through life, he fills in a number of forms for the records, each containing a number of questions.... There are thus hundreds of little threads radiating from every man, millions of threads in all. If these threads were suddenly to become visible, the whole sky would look like a spider's web...."

As those webs grow, whether they contain threads of personal or business information, it becomes increasingly difficult to locate a particular item. For example, if you are researching a topic, you might start the search in the Reader's Guide to Periodical Literature, an index to articles that have appeared in 200 popular consumer magazines. But if the subject might also be covered in technical journals, you will have to check reference works similar to the Reader's Guide that cover the subject. If you are not familiar with those reference works, you must take an additional step away from the material you seek and look into something like The New York Times Guide to Reference Materials. In other words, even the number of information cross-references is so large that we need a "guide to the guides."

Each information level we are forced to transcend in search of a fact lessens the desire to perform the search in an inverse square proportion. If a related fact is two levels away, we're one-fourth as likely to make the effort to track it down; for three levels, it's one-ninth as likely (Reference 9).

HyperCard also has what a database management devotee would call "relational capabilities." That's because information stored in one stack of HyperCard forms can be retrieved by forms in other stacks. HyperCard takes quite a large additional step, however. Unlike a relational database, HyperCard actually lets you zip over to other stacks to view the full context of related information. Thus, while a relational database generally restricts its relational capabilities to simply retrieving information from elsewhere, HyperCard lets you hop around as your information needs require.

Nor are the links you establish finite or rigid. You can adjust the links as you please or create new ones as additional files of related information are added to your collection. The threads, in other words, can keep growing and weaving, like an ever-expanding spider web (Reference 10).

The greatest impediment to progress in the Information Age is ineffective navigation techniques in the quest for relevant but widely dispersed knowledge. Now that we have the technology to overcome this obstacle, it is our responsibility to make the investment necessary realize the remarkable vision of our early information pioneers.

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THE "TOOL BOX" APPROACH FOR MANUAL ASSEMBLY OR REPAIR OF THRU-HOLE AND SURFACE MOUNT DEVICES

by

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ABSTRACT

This paper traces the evolutionary changes in the equipment and techniques used for manual assembly or repair of surface mount devices. It discusses two approaches used in the past and presents a third "Tool Box" approach. Each approach is compared in its ability to satisfy requirements of Versatility, Process Control, and Safety. Critical requirements for handpieces and controllers are also discussed as a part of this paper.

INTRODUCTION

The evolution of surface mount technology created new assembly and repair problems and challenges. A new set of processing steps and techniques had to be developed to handle surface mount devices because of their mounting characteristics, smaller lead size, greater lead count and other related parameters. These steps are summarized in Table 1 for both initial assembly and repair and contrasted with thru-hole technology.

Historically, thru-hole technology went through an evolutionary stage during which the tools and techniques for assembly and repair were developed. In the manual assembly area, the most notable advance was the progression of the soldering iron from a relatively uncontrolled and bulky device to a modern closed-loop, lightweight handpiece. In the repair area, the major advancement was the continuous vacuum desoldering handpiece which revolutionized component removal. Prior to these developments, thru-hole assembly or repair were more difficult to accomplish in a repeatable, process controlled fashion.

A similar evolution in tools and techniques has already taken place in surface mount production assembly. In the production area, a completely new set of automated manufacturing equipment is now used. For example, Infrared and Vapor Phase reflow systems have generally replaced the wave soldering apparatus which was standard in thru-hole applications. Likewise, solder creams have become the successor for molten solder. In the manual assembly and repair areas, the same progression has been taking place. This paper will focus on the changes in these areas by describing various techniques which are used to remove and install surface mount components and indicating those approaches which provide the greatest versatility, safety and process control.

OBJECTIVES FOR MANUAL ASSEMBLY OR REPAIR

It is fairly easy to establish restricted requirements for manual or semi-automated equipment based solely on limited information or experience. For example, if only one pc assembly and one or two components are considered, the assembly or repair equipment can be very specific, and quite possibly, highly automated. Normally, however, most equipment for manual and semi-automated assembly or repair must be designed for use in many scenarios as indicated by Table 2. If one considers the needs of these areas, a set of goals for any piece of surface mount equipment can be developed. There are three primary goals for this equipment, namely:

VERSATILITY

Versatility is an all encompassing phrase, but in this instance it generally means that the following criteria are satisfied:

Installation and Removal of Any Component

This is a pretty tall order for any system, because of the variety of component types and sizes currently availableand the many new component shapes still under development. Nevertheless, the equipment which best achieves this aim will have the greatest use in all the areas described in Table 2.

Size, Complexity and Cost

In some of the areas in Table 2, size, weight, and the need for special services (i.e., shop air or high current) are serious considerations. Equipment which relies on the fewest external support services for proper operation are generally the most versatile. Likewise, complexity of operation can also determine whether a piece of manual assembly or repair equipment is useable on any bench top or requires a dedicated area in a facility and a highly trained operator. Cost is not a performance factor, however, as more small and middle size companies enter into surface mount technology, the relative cost of all equipment is a key consideration. Equipment which delivers the greatest utility for the purchase and operating cost will receive the widest use.

CONTROLLED PROCESS TECHNIQUES

Many companies have devoted extensive time and considerable resources to establish modern surface mount production facilities. New manufacturing engineers or consultants are often hired to establish and control the production processes, and frequently, a significant financial investment is made in automated paste deposition, pick and place, solder reflow and pcb cleaning equipment. In manual assembly, however, operators are often given little more than a soldering iron to carry out essentially the same tasks and achieve the same results as the automated production area. In repair, the problem is even more difficult since the board is fully assembled and needs to be carefully de-manufactured before being re-manufactured. The concept of process control in repair is often talked about but not generally given the attention it truly deserves. In fact, the manual assembly or repair of surface mount assemblies requires the same care and understanding of the process as in the production area to achieve the best results.

To guarantee that manual or semi-automated processes occur in a controlled manner means that the following conditions must be met:

a. There must be a well-defined set of relatively simple steps in the process. If the number of steps is too large, the operator may inadvertently omit one or more of them.

b. The steps must be easily and consistently carried out by trained operators with reasonable skill levels. Even the best set of steps will not lead to process control if the steps are too difficult to be achieved.

c. The tools used by the operators must be designed with process control and human dexterity in mind, and ideally should minimize critical aspects of the tasks. This further guarantees that the task can be accomplished at a reasonable skill level. In fact, as the design of the equipment improves, the reliance on critical human skills should be reduced.

SAFETY

Simply stated: The assembly or repair process must cause no physical or thermal damage to the component, substrate or adjacent components.

The Component

When semiconductor devices pass through an IR or Vapor Phase reflow cycle, the die normally achieve temperatures of 200°C or more. Tab components and other assemblies which use solder in the die attachment process may limit maximum die temperatures to 150°C during production to prevent damage to the component assemblies. Hot bar, laser or other similar techniques are frequently being used to assure staying below 150°C during production. These maximum component die temperatures serve as useful guidelines for the appropriate manual assembly or repair processes to suit the same family of semiconductor devices.

Other components, such as ceramic chip capacitors, may be able to accept relatively high temperatures but the rate of temperature rise and thus, the rate of heat application is the critical factor to avoiding thermal shock. Process techniques in both assembly and repair must therefore include some method of preheating to safely install or remove these devices.

The Substrate

Depending upon the composition of the substrate material; the rate of heat delivery, the type of tools used, and the need for preheating or bake-out are all necessary considerations. Otherwise, board warping, measling, lifted tracks or other damage can occur.

Adjacent Components

Perhaps the least understood of the safety criteria is the potential damage to adjacent components which can occur during an incorrect manual assembly or repair task. In production, an entire assembly is reflowed at once and adjacent reflow is not a consideration. Perhaps this is why it is often ignored during manual assembly or rework. Generally, the repair process should insure that adjacent solder pad temperatures are kept below 150°C to insure that no degradation occurs to these solder joints in the form of intermetallic growth, crystallization and embrittlement. In fact, this consideration is one of the critical factors in determining which manual or semi-automatic techniques are best suited for a specific component removal or installation.

APPROACHES TO SURFACE MOUNT REPAIR

In recent years, two approaches have been popular for manual assembly and repair, and more recently a third approach has evolved. These will be considered along with their merits and limitations. In this paper they will be referred to as: The Large Machine, the Single Tool and the Tool Box approaches.

LARGE MACHINE APPROACH

At the onset of surface mount development, the design and repair tasks at first seemed difficult if not insurmountable. Only a few years ago there was a continual debate about all the problems of handling 50 mil component spacing. Now the discussion is about 25 mil or smaller spacing, and 50 mil parts are accepted as commonplace by most manufacturers.

The early impression of difficulty led many manufacturers to assume that manual assembly or repair tasks could no longer be accomplished by human operators, and led to the development of many specialized hot gas and hot bar placement and removal stations for surface mount assembly and repair. These machines satisfied most of the acceptance criteria. For example, the best machines:

a. could handle a wide variety of components;

b. allowed a controlled process approach to assembly and repair with easily defined and repeatable steps which could be followed by trained operators with reasonable skill levels; and

c. considered safety criteria by, for example, controlling the rate and location of heat flow to avoid physical and thermal damage to components and substrates.

As the development of surface mount technology progressed, the concept of a large machine as the only solution has been challenged. It has been proven in many instances that human operators with hand tools can perform the same tasks as hot gas or hot bar machines with comparable results. This has led some companies to depart from the machine approach as the sole technique for manual assembly or repair. Furthermore, the large hot gas or hot bar reflow machine is often an expensive solution and is typically part of a dedicated facility used only by a few trained operators. This could present an inconvenience in contrast to the less expensive, readily available manual repair or assembly techniques so common with thru-hole components. These considerations have prevented the large machine from becoming a universally accepted solution.

THE SINGLE HAND TOOL APPROACH

The second approach to surface mount repair came about by human ingenuity in extending the use of available hand tools, the most common of which is the soldering iron. This handpiece was quickly applied to surface mount tasks by adding special tips which allowed the handpiece to evolve from a single point (i.e., solder joint) to a multi-point reflow tool. Tips for the removal of chip components, and SOICs quickly evolved and are shown in Figure 1. When the tip fit the task, the application worked well and both process control and safety parameters were satisfied.

In other cases, the evolution became strained and often continued into areas where safety and process control requirements could not be satisfied. For example, tips for conventional soldering irons have been developed for the removal of PLCCs. In this instance, no provision has been made for providing the best delivery of heat to the lead/land area or lifting of the component after reflow. Such limited tools often complicate the task, thereby compromising the safety of the assembly or repair process.

Another approach in recent years has been the use of hand-held hot air handpieces as a universal tool for removing and replacing all surface mount components. The tool has some valuable uses, but fails to consistently meet safety and process control requirements. For example, the hand-held systems often lack the vacuum pick-up capability of larger machine systems, and component removal requires two-handed procedure. This may seem trivial, but often makes the removal task considerably more difficult to safely accomplish.

The most critical limitation of the hand held hot air approach, however, is in the safety area. The air temperature, time of reflow and direction of air flow are often poorly controlled, compromising safety criteria. Specifically, adjacent components are often heated beyond the 150°C guideline. Quite frequently, the tool is applied indiscriminately, and the substrate is overheated producing warping or measling. An example of improper removal is shown in Figure 2 where thermal data on the reflow of a flatpack with a hand-held hot air tool is indicated. It clearly shows that adjacent components 0.100 inches away exceed the 150°C guideline. While it is possible to remove the component safely, the conditions in Figure 2 can occur unless the tool is used with absolute precision. Maintaining this precision is possible but not easy, even for trained operators. Thus, while hot air may have a use, it cannot solve all problems in a safe, reliable manner.

THE TOOL BOX APPROACH

This approach is based on the old sound principle of using the appropriate method to suit the specific job. It basically includes a set of handpieces designed to safely accomplish specific tasks in much the same manner as a garage mechanic uses a full set of specific tools to repair a car. Each tool has a defined purpose and is specifically designed to carry out that purpose. In order to create this "tool box" some basic thermal guidelines are followed.

1. Use conductive heating devices for component removal and specific installations

Hand-held, conductive (heating by contact) tools are better at targeting heat on the solder joints than comparable convective (heating by gas/air flow) tools. This generally means that conductive devices can be used by operators for multi-leaded component removal without concern about unduly heating adjacent components. Contrast the unsafe convective removal in Figure 2 with the removal of the same component in Figure 3 using the conductive device shown in Figure 4. Notice that the conductive device quickly removed the component while transferring very little heat to adjacent components 0.100 inches away. Notice also that the process is accomplished so quickly that the internal die temperature remains quite low. This process is not only safe for present day flatpacks, but potentially safe even for newer TAB components.

Single point, conductive tools are also useable for component installation and many straight and bent small point coined and chisel tips are utilized for this purpose. With practice, the task can be accomplished by most operators. In many instances, such as with surface mount sockets whose leads are hidden and fine pitch quad flatpacks, solder bridges or inadvertent damage to the plastic portion of the package can occur. In such cases, fine point convective tools often work better.

2. *Use tools designed to supply heat at lead/land areas*

The handpieces must properly be designed for the specific application and target heat at the lead/land interfaces. For example, Figure 5 shows two conductive tools for the removal of PLCCs. In 5A, the device merely fits into an ordinary soldering iron, and attempts to slip over the component. Because of the need to clear the top of the PLCC body, the best this device can do is to provide heat at the shoulder of the leads which is eventually carried down to the pad area. The process, as might be expected, is slow. In 5B, a tweezer approach allows the tip to be slipped over a component and then squeezed together to direct heat much more directly and quickly into the lead/land area. The performance comparison between these two approaches is shown in Table 3. Note that the tweezer often removes even the larger PLCC packages in less than 10 seconds, whereas the soldering iron adapted tip requires nearly a minute for the same task.

3. *Use convective tools for replacement*

Convective tools have advantages in component replacement since they provide a non-contact process. To minimize the danger of overheating adjacent components, the heating system must be focused. It should also provide heat only on demand to avoid inadvertent damage while preparing to replace a component. Figure 6 shows a focused convective tool replacing an SOIC using a scanning technique and Figure 7 shows the thermal characteristics of the reflow process. Again, the process is delivering heat in a controlled manner and causes no damage to either the component, substrate or the adjacent devices.

4. *Use operator friendly tools*

The specific tools must be designed with the user and application in mind. For example, one-handed operation with these tools greatly simplifies the task and helps guarantee success. Thus, each removal tool should not only properly heat the component, but must also be able to lift the component after reflow. For flatpacks, a vacuum pick built into the handpiece insures this; while for PLCCs, the tweezer design accomplishes the heating and lifting task. For smaller components such as chip devices or SOICs, a special tip in a soldering iron (such as shown in Figure 1) or tweezer tips may be used. With the soldering iron tips, the surface tension of the solder between the tip and component is usually adequate to lift the component away with the tool once reflow occurs.

With hot air tools, the task is made easier if the rate of air flow or (exit air velocity) is kept low enough to avoid disturbing the part. Many hot air systems can actually blow small components off the pc assembly and require the operator to secure them with a tweezer or vacuum pick. This action can disturb the component after the solder has achieved reflow, creating an unacceptable solder joint. For one-handed operation, a low air flow system does not require securing the component and makes the task easier and more reliable.

COMPONENTS OF THE TOOL BOX

Specifically which combination of tools works best can be debated, and some alternatives to the following list might be suggested. A combination which is being used successfully in process-controlled applications is contained in Table 4. It contains the following elements:

1. A high-quality, closed-loop soldering iron for thru-hole soldering, and removal of chip and SOIC components.

2. A solder extractor, for normal desoldering applications.

3. A specialized "flo" desoldering handpiece to remove old solder from surface mount lands. The removal of solder from land areas with a continuous vacuum provides a safer, less costly and convenient one-handed alternative to the use of solder wick.

4. A thermal tweezer for PLCC and LCCC removal. This device may alternately be used for removal of chip and SOIC components.

5. A thermal heating device with a built-in vacuum pick for the removal of extended lead components such as flatpacks and PQFPs.

6. A low velocity hot air jet device for the installation of all types of surface mount components.

It is possible that additional tools will be included in the "tool box" as new applications occur, but for the moment, the present array allows nearly any surface mount or thru hole device to be assembled or replaced safely and effectively by operators with minimal training and skill level.

THE INTEGRATED POWER SOURCE

The above array of tools can be realized by combining a variety of different products. Considering the limited bench space in a modern assembly or repair area, it is often better to combine the elements required to support these handpieces into an integrated power source. The power source must provide closed-loop temperature control to allow accurate setting of initial tip temperatures and to insure proper heat delivery in response to load requirements. It should also be multichanneled and capable of driving multiple handpieces at a time. This may not be obvious, however, anyone who assembles or repairs surface mount thru-hole assemblies will have to switch between tools more frequently than was required with thru-hole assemblies. Thus having multiple handpieces available at a moment's notice is quite desirable. In repair areas where a component must be removed, the substrate cleaned and the component replaced, the ability to have multiple handpieces readily available is even more apparent. The self-contained power source should also ideally provide the air, vacuum and controls required by the tools.

CONCLUSION

The array of handpieces and the modern multichannel controller form the basis for the box of tools required for manual assembly or repair of all surface mount and thru-hole components. It satisfies the criteria of versatility, process control and safety in a relatively low cost configuration. It therefore can provide the desired functions to more users than the large machine approach because of its smaller size and lower cost. Alternately, it yields better results than single tool approaches, because of its ability to use a variety of tools designed for specific purposes. For many companies who are presently working or planning to work with surface mount technology, this is a powerful approach to consider.

MAJOR STEPS IN THRU HOLE AND SURFACE MOUNT ASSEMBLY AND REPAIR PROCESSES

ORIGINAL ASSEMBLY

THRU HOLE	SURFACE MOUNT
1. INSERT COMPONENT IN HOLE	1. APPLY SOLDER PASTE
2. WAVE SOLDER	2. TARGET, ALIGN AND PLACE COMPONENT
3. CLEAN PC ASSEMBLY	3. REFLOW PC ASSEMBLY
	4. CLEAN PC ASSEMBLY

REPAIR

THRU HOLE	SURFACE MOUNT
1. DESOLDER OLD COMPONENT	1. UNSOLDER OLD COMPONENT
2. REMOVE OLD COMPONENT	2. REMOVE OLD SOLDER
3. CLEAN PC ASSEMBLY	3. CLEAN PC ASSEMBLY
4. INSERT NEW COMPONENT	4. TIN PADS AND LEADS OR APPLY SOLDER PASTE
5. SOLDER NEW COMPONENT	5. TARGET, ALIGN AND PLACE NEW COMPONENT
6. CLEAN PC ASSEMBLY	6. REFLOW NEW COMPONENT
	7. CLEAN PC ASSEMBLY

TABLE 1

AREAS WHERE SMD MANUAL ASSEMBLY OR REPAIR EQUIPMENT IS UTILIZED

1. REPAIR OF PRODUCTION FAULTS
2. DEPOT REPAIR
3. FIELD SERVICE
4. DESIGN CHANGES
5. PROTOTYPE DEVELOPMENT
6. SHORT RUN PRODUCTION

TABLE 2

CHIP AND SOIC TIPS FOR USE WITH STANDARD SOLDERING IRON

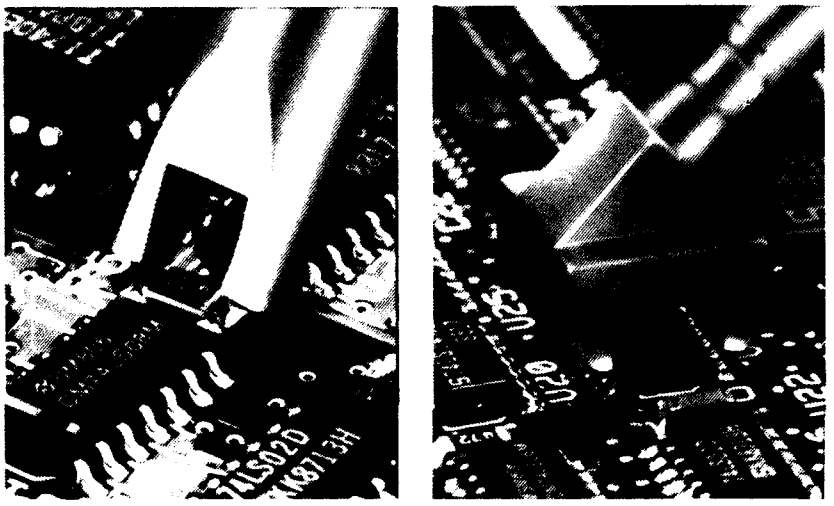

FIGURE 1

REMOVAL OF 67 PIN FLATPACK WITH HAND-HELD 4 SIDED CONVECTIVE TOOL

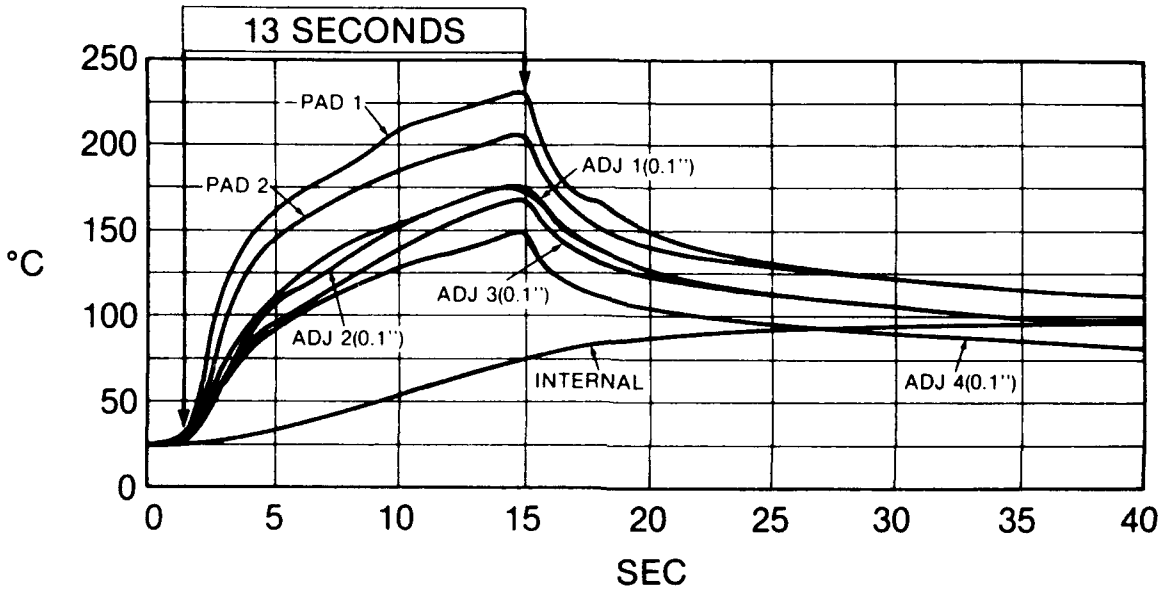

FIGURE 2

REMOVAL OF 67 PIN FLATPACK WITH HAND-HELD CONDUCTIVE TOOL WITH BUILT-IN VACUUM PICK

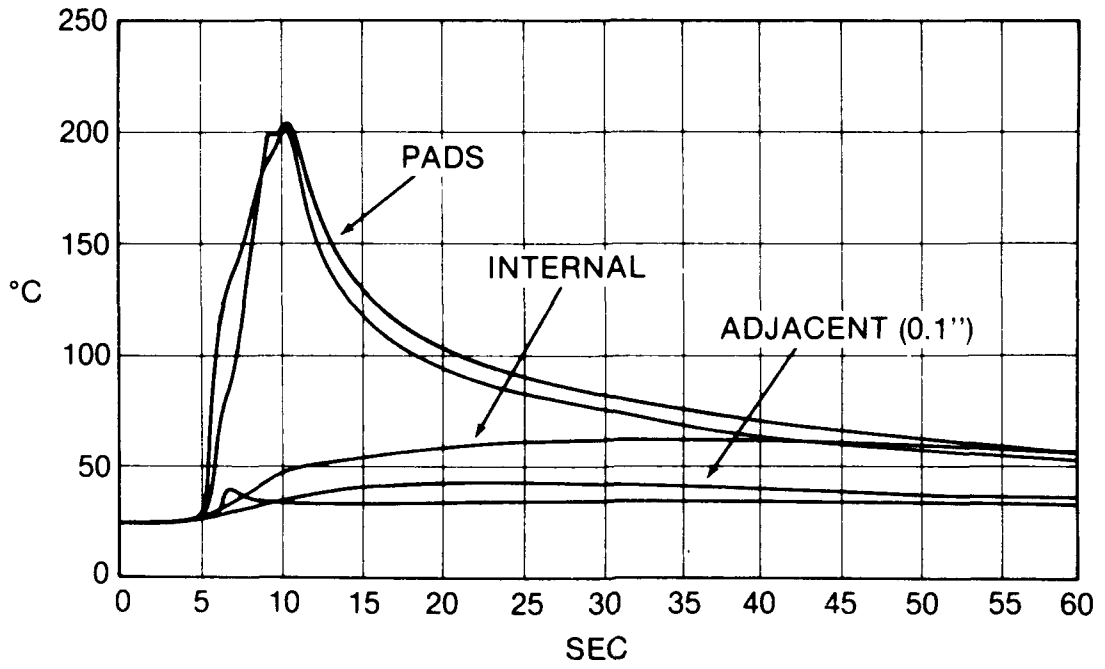

FIGURE 3

CONDUCTIVE TOOL WITH BUILT IN VACUUM PICK

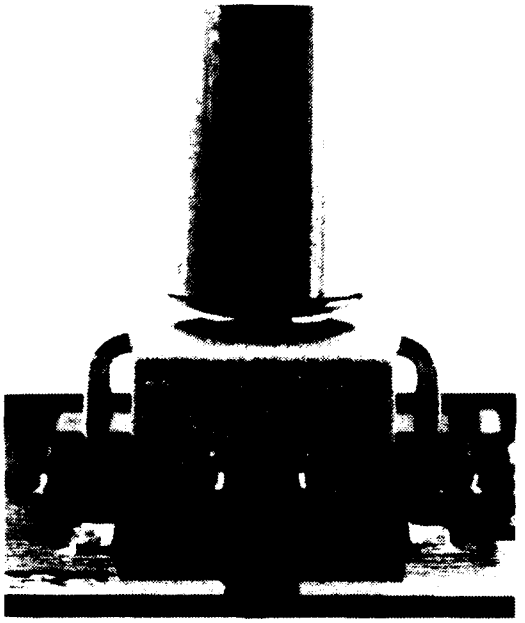

FIGURE 4

COMPARING PLCC REMOVAL DEVICES

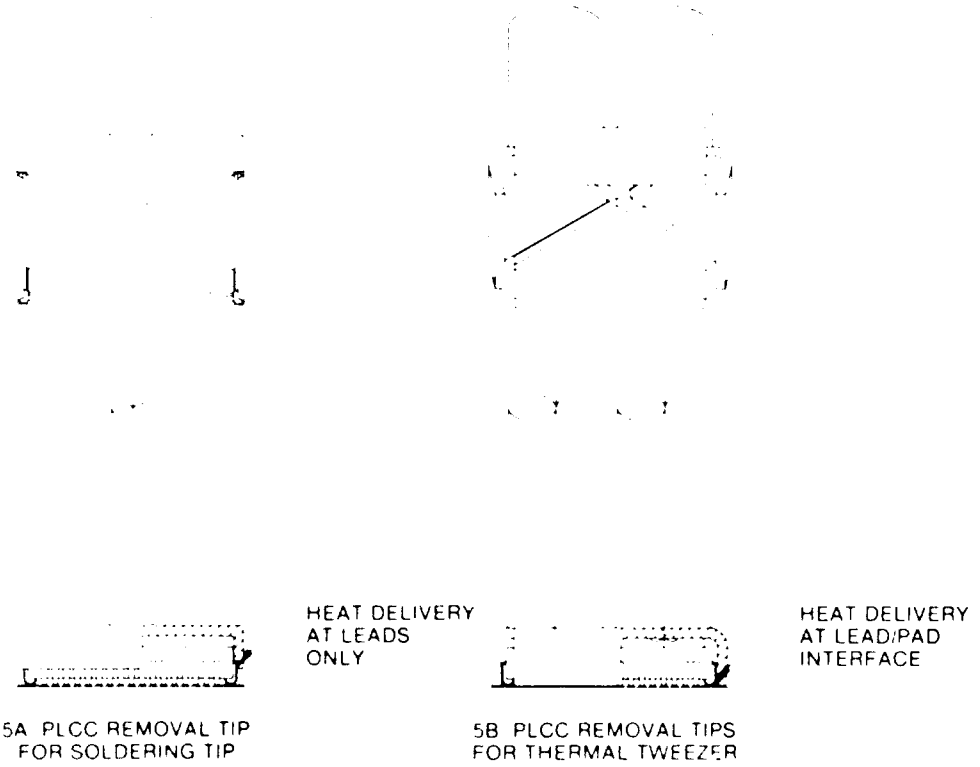

FIGURE 5

COMPARING COMPONENT REMOVAL TIMES

COMPONENT	THERMAL TWEEZER	SOLDERING IRON TIP
20 PLCC	2-4 SEC	-----
44 PLCC	4-6 SEC	15-20 SEC
68 PLCC	5-10 SEC	55-60 SEC
84 PLCC	7-12 SEC	-----

TABLE 3

REPLACEMENT OF SOIC WITH CONVECTIVE MINI HOT JET WITH FOCUSED BIFURCATED TIP

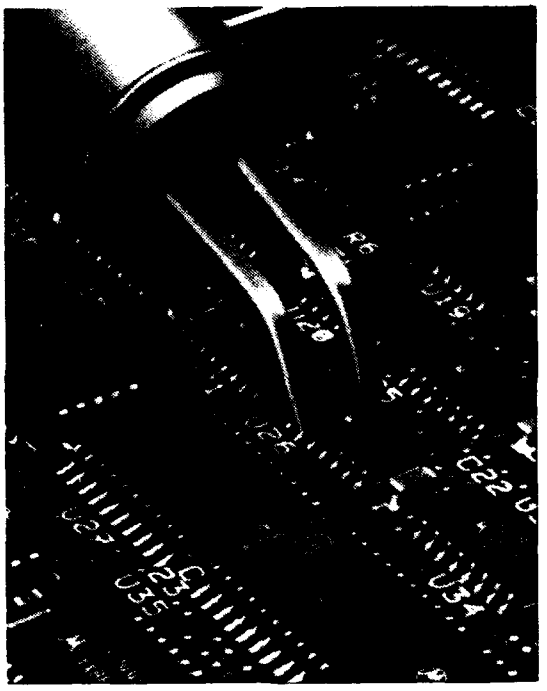

FIGURE 6

MINI HOT JET REPLACEMENT OF SOIC

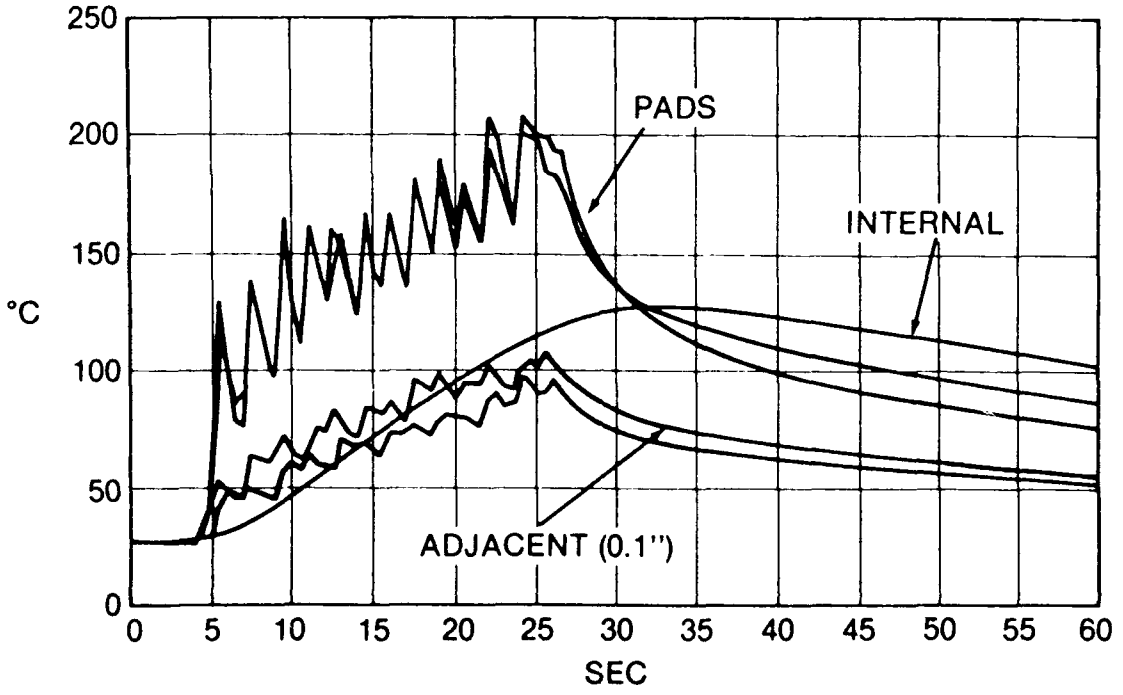

FIGURE 7

ORGANIZATION OF THE TOOL BOX

TASK	PREFERRED HANDPIECE	TIP
REMOVE CHIP COMPONENTS	SOLDERING IRON	CHIP TIPS
REMOVE SOICs	SOLDERING IRON	SOIC TIPS
REMOVE PLCCs	THERMAL TWEEZER	PLCC TIPS
REMOVE LCCs	THERMAL TWEEZER	LCC TIPS
REMOVE FLATPACKS/PQFPs	THERMAL PICK HANDPIECE	FLATPACK TIPS
THRU HOLE REMOVAL	DESOLDERING	SIZED TO PAD
SURFACE MOUNT SOLDER CLEAN UP	FLO DESOLDERING	FLO TIP
SURFACE MOUNT PAD TINNING	SOLDERING IRON	TINNING TIP
COMPONENT REPLACEMENT WITH SOLDER PASTE	THERMAL JET	SMALL FOCUSED TIP
COMPONENT REPLACEMENT WITH SOLDER	SOLDERING IRON	MINI TIPS

TABLE 4

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Louis is a Fellow of the Audio Engineering Society, and author of numerous papers on audio, acoustics, engineering design, and rework and repair. He is a member of the technical committees of AES, EIA, IPC, and ISO.

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SPIN TINNING
A NEW PROCESS TECHNOLOGY

by

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ABSTRACT

Spin tinning is a new alternative to solder dip tinning for surface mount components. Test results on leadless chip carriers and photomicrographs of leaded chips are shown. The interaction of final velocity versus acceleration as they affect tinning results are now better understood and discussed. The photomicrographs also display the variations in tinned coatings and the effect of spinning on the solder coat. Costs are discussed and displayed as a variable by labor rate in dollars versus production rate. Tinning costs can be expected to be in the five cents to ten cents per component range.

INTRODUCTION

Surface mount devices (SMD's) differ from through hole components in many obvious ways, dictating different handling and assembly techniques and machinery. Each successive year SMD's are becoming more commonly used while simultaneously the scale of component integration becomes higher, their physical size smaller, their lead pitch finer, and the number of configurations available multiplying. Because of their very reduced scale, SMD's are much harder to solder to their fine trace printed circuit boards (PCB's) and the quality of the solder joint more difficult to inspect and repair. New lines of specialized machines have been developed specifically in support of SMD's and SMD assembly.

Through hole components give the PCB designer a realistic physical limitation when downsizing PCB's. The solder joint fillet, both top and bottom, has a minimum physical size that results in a practical bottom limit of about .050" spacing. Dual-inline-packages (DIP's) are an often used packaging method for through hole integrated circuits. They are commonly .100" lead center to center distance, four to twenty plus leads, tin plated, and usually handled in plastic tubes.

The DIP depends upon its PCB hole design and quality, as well as its solderability to achieve a good solder joint. Hot solder dipping (tinning) the leads of a through hole component such as a DIP enhances its solderability and gives the component extended shelf life. Generally through hole components are less complex than the more highly integrated SMD's and therefore less costly. Through hole components are usually tinned with the attendant extra cost only if there is a need to ensure solderability or long life - e.g., military applications. Tinning through hole components is more of an art than a science because of the variety of types to be tinned. However, the margin for quality error is fairly broad because of relatively large lead size and the solder fillet geometry.

Surface mount components are a more demanding component and tin dipping becomes more important for several reasons. Tinning SMD fine pitch leads not only increases the

SMD's solderability to PCB fine traces, but also significantly aids in minor coplanarity problems and especially in allowing a larger margin of error in the placement and amount of deposited solder paste. As previously noted, SMD's are frequently a more complex device than a through hole component and, therefore, more expensive; justifying hot solder lead tinning for purely commercial reasons.

Through hole components are tinned using primarily the force of gravity to remove excess solder, though air knives are sometimes added as an additional aide in removal.

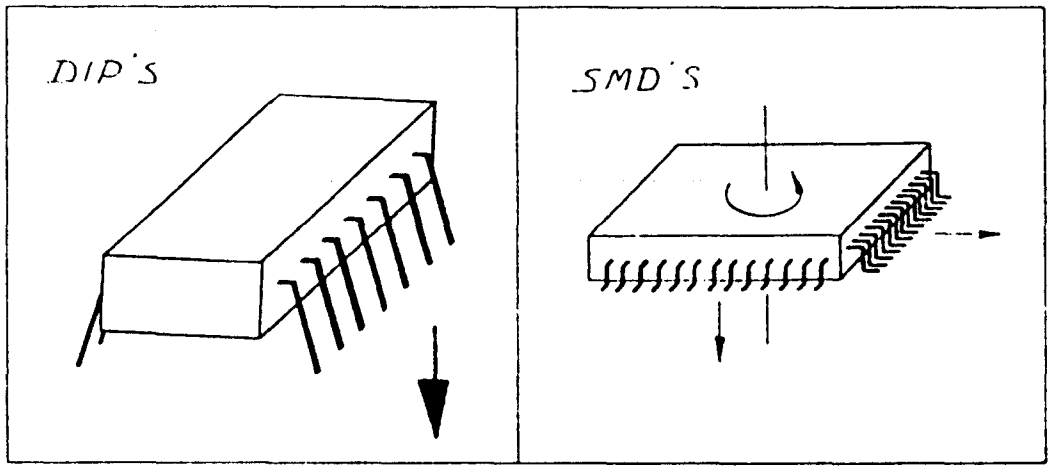


Figure #1
Comparison of DIP's dependency on gravity for excess solder removel verses centrifugal force for spin tinning SMD's

The thickness of solder is therefore somewhat consistent despite the size of the tinned lead. This thickness is typically .003" to .005" with a variation in quality and a tendency to have problems caused by the final "drip off" of the solder.

Unit Design conceived of using centrifugal force as the solder removal force in 1986 and commenced experimentation of this new process technology. Figure 1 shows the graphic comparison of the basic solder removal differences. The obvious advantage of using centrifugal force for excess solder removal is the fact that the force can be controlled. However, the process technology depends upon controlling some combination of acceleration and final velocity. Experimentation focused on this area.

SMD's typically have leads on two or four sides and can be divided between leadless chip carriers (LCC's) and leaded chips. Our tinning tests have shown that there is a dramatic difference in processing requirements between the two types of leads. In addition to the obvious dissimilarity of the LCC's flat metal plate lead flush with the component body versus an extended wire form such as a gull wing or "J" lead, the LCC's are frequently gold plated, making gold scrubbing prior to final tinning desirable.

The more common leaded gull wing and "J" SMD's are components with a greater need for hot solder tinning. The center to center spacing, or pitch, of these types of leaded components have progressively gotten finer and finer; from .050" to .025" to .020". Some extra fine pitch SMD's are now below the .020" level, testing the physical limits of the SMD process just as the limits of the through hole process was reached.

EXPERIMENT AND ANALYSIS

Our first experiments by M. W. Tanny used a Unit Design ALT-100 lead tinning system to supply the basic tinning process and mounted a rack of controllable motors to hold and spin the SMD's. The collets used were magnetic and had raised barriers on the periphery to physically contain components in case of misalignment. This severely limited the types of SMD's that could be tinned to chips that a e magnetic; commonly leadless chip carriers.

Our experiments fixed the SN63 solder temperature at 500 degrees F., preheated the LCC over the solder pot for thirty seconds to primarily dry the flux (achieving about 130 degrees F.), set the solder exit pause time at 0.5 seconds, and spun the LCC for 0.8 seconds. The motor was programmed to rotate slowly while in the flux and in the solder for scrubbing. Rectangular LCC's were chosen for the experiment to determine impact of major and minor lengths. The LCC's were gold plated when received and the height of the gold plated lead above the ceramic body was measured at .00057" average height. LCC's were spun at a series of speeds beginning at 2,000 RPM, increasing at 500 RPM increments. The maximum speed achieved was 7,000 RPM.

Two bands of speed showed consistent results, while the other speeds produced wide variations in results. Figures 2 and 3 show these two areas where satisfactory results were obtained, 4,000 RPM and 6,000 RPM.

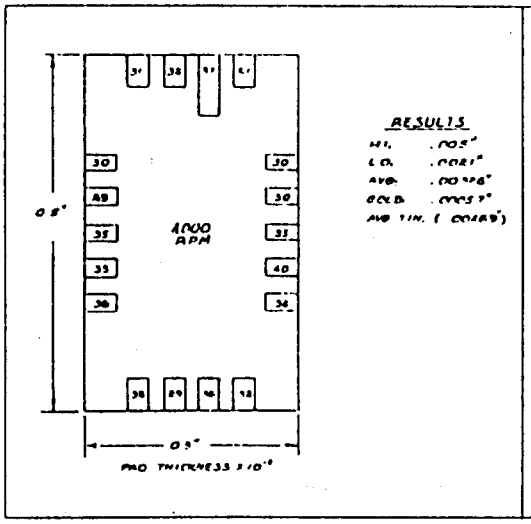


Figure #2
Tinning thickness on LCC leads
@ 4000 R.P.M.

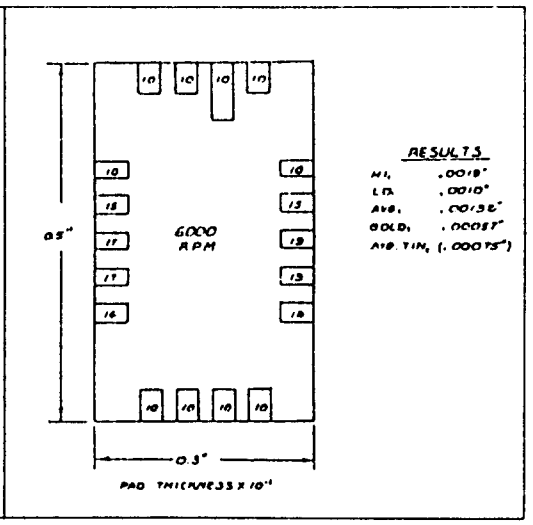


Figure #3
Tinning thickness on LCC leads
@ 6000 R.P.M.

The major and minor length differences did show solder thickness variation, as expected, but less than anticipated. The 4,000 RPM regime can be used for solder coating, where excess solder is wanted on the flat leads. The 6,000 RPM regime is the speed of solder plating. Our observations showed that G force was the dominant factor, taking into account the LCC length and final RPM. The formula used is G = length x RPM x 100.

Results

1. Below 10 G solder deposits on LCC pads were as inconsistent as regular dip tinning with large globules on some pads (.008" to .020") and marginally acceptable globules on others (.002" to .005").

2. At about 10 G solder deposits of .002" to .004" can be maintained on all pads.

3. Above the 10 G band results again became inconsistent with some pads at the .002" to .004" range and some at .0003" to .0005" thickness.

4. At the 20 G band all pads were tinned to the .0003" to .0005" thickness.

The same process was then extended to leaded SMD's with mixed results. LCC leads are imbedded in a base which initially is a heat sink when placed in the hot solder. As the LCC is removed, the LCC base functions as a heat reservoir and slows down the lead cooling when removed from the hot solder. Solder exit pause times are less critical and the rapid cooling effect of spinning are partially negated by the LCC functioning as a heat reservoir.

One important piece of information was developed, however. By fixing the spin duration at 0.8 seconds, and determining that G is the critical factor, we were pointed in the right direction in determining the importance of acceleration versus final speed. Further experiments showed that acceleration becomes the dominant control factor for leaded chips, especially for fine pitch. The other ten plus variables ranging from solder temperature to lead diameter are contributory to the final process settings, but not as critical as acceleration. This new process technology can be used relatively easily without serious concern for most variables.

There is a predictable phenomena regarding the actual solder coating. Any vertical portion of a lead will have its solder coating displaced to the outside of the lead.

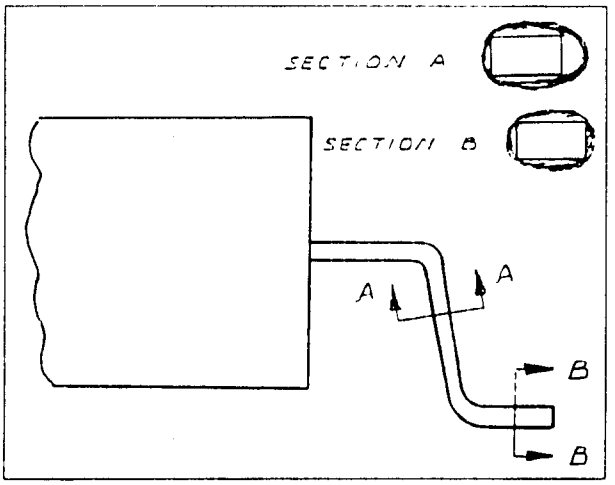
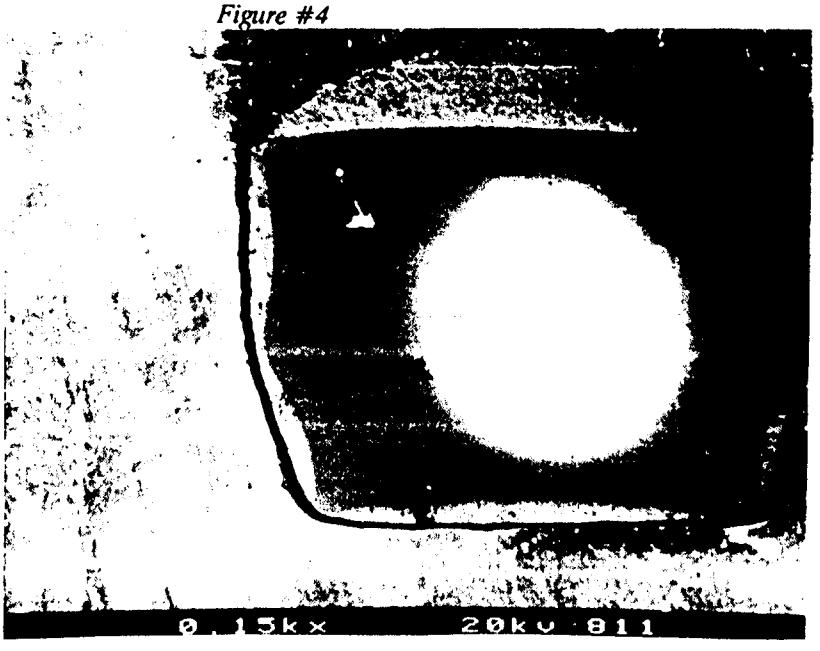


Figure #4

Figure 4 shows the theory of this offset of the coating graphically and Figure 5 is a microphotograph of a vertical section of a gull wing terminal.

Figure 4 and Figure 5 also illustrate another forecastable phenomena. The surface tension of the hot solder rounds off square corners on square or rectangular cross section leads. The solder coating literally smooths out the metal lead irregularities as shown in the photograph, Figure 5. Though the whole lead surface is coated with hot solder, it cannot be uniform. This could cause a problem to those companies and agencies that wish to control supplier quality by setting solder thickness standards for tinned leads.



Two machines are now available in the United States to provide this new process. Both have one station for manually unloading/loading and leave the remaining station's function up to their potential customer. One was initially designed as a gold scrubber and devotes two of its three remaining stations to

two solder pots. Gold scrubbing is accomplished by rotating the component in the static solder pots.

The other machine has five stations available for precleaning, fluxing, preheating, solder coating, gold scrubbing, cleaning, and rinsing. The general layouts of the two machines are shown in Figure 6 as machine A and B.

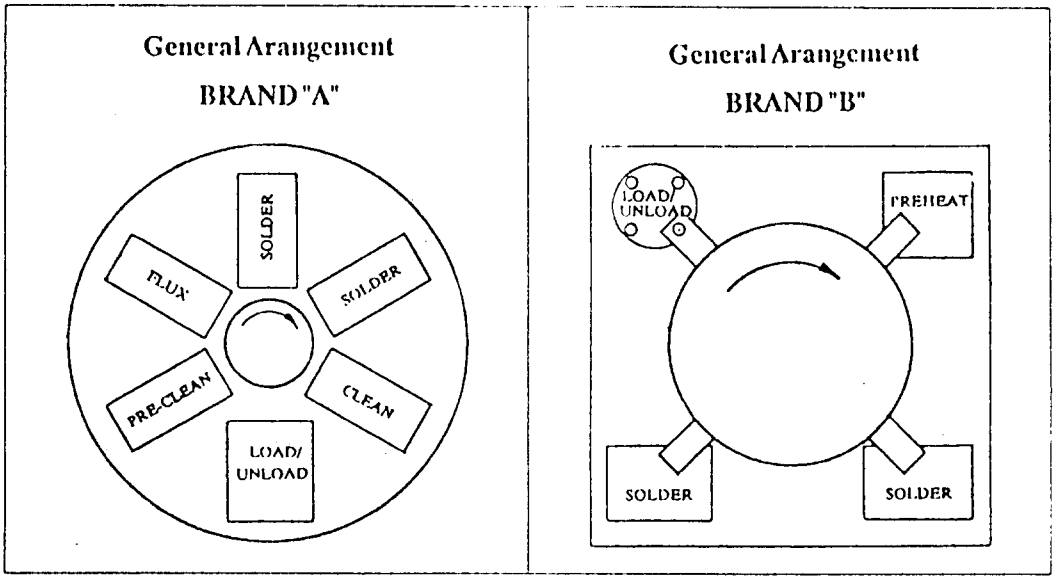


Figure #6
Brand "A" *Brand "B"*

COSTS

Does this new process merit consideration? Only if the product improvement is worth the additional cost. To tin the leads of a relatively inexpensive component would only be acceptable if solderability and/or coplanarity was critical. However, the component manufacturer would still not be interested in increasing his manufacturing costs by adding another process step unless there was some clear gain to be realized from adding this step. The component manufacturer is interested in solderability and coplanarity, but not to the extent the board assembler is concerned.

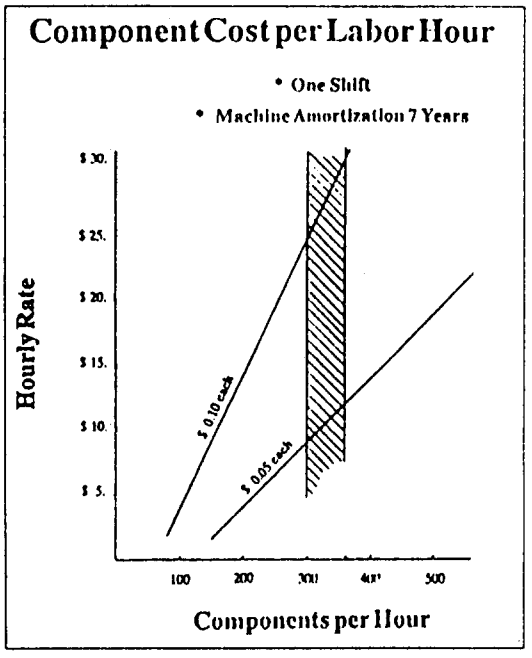


Figure #7

To analyze the cost of tinning components, three inputs are critical: the burdened labor cost per hour, the throughput and the machine cost. There are other important cost-contributing factors such as consumable material costs, maintenance costs, number of shifts, level of training required,pre and post tinning handling, etc., but for simplification, we will use the first three factors as the most dominant in costing, approving, and selecting the process and equipment. By fixing the machine cost at $12,000/year using a 2,000 hour shift year, seven shift years will produce

a fixed cost of $6.00 per hour. We will treat the hourly rate and components per hour as the two variables and generate the cost graph as Figure 7, which has already had the cost lines displaced to include the $6.00 machine cost.

The area of interest is the 300 to 360 components per hour band, based upon an anticipated throughput of ten to twelve seconds per cycle. In a low labor rate area such as Mexico or Southeast Asia, the component tinning cost is about $0.05. In the United States, the higher labor costs and burden will cause tinning costs to be closer to $0.10 each. It would be unlikely that a component costing $0.86 would be tinned, unless there are other compelling reasons. However, a quad pack costing $23.00 would merit such usability enhancement.

John Abouchar is President of Unit Design, Inc. He has had 6 years of experience in soldering and tinning process machines. He holds a BSME degree from Stanford, and has a patent on a mass flow meter with reduced attitude sensitivity.

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